Performance Analysis of 16-Bit qALU using Reversible Logic Gateswith QCA for Quantum Processors

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Abstract:
The NAND, NOT, and NOR logic gates which are utilised to realise the hardware modules of the system, are examples of basic classical logic gates that make up the hardware basics of electronic circuit systems. In addition to this, a useful system has been described for designing and implementing quantum processors by using reversible logic gates to analyse the performance of ALUs. Additionally, it shows that QCA might be used in quantum computers, assuming that the underlying technology can be made workable. When considering energy-efficient computations, reversible or information-lossless circuits are crucial for digital signal processing, communication, computer graphics, and cryptography. By preventing information loss, reversible logic is utilised to lessen the power dissipation that occurs in classical circuits, which is particularly promising because it allows for extremely low power computations like nano-computing for quantum processors. Because bits of information are lost during logic operations, typical digital circuits waste a lot of energy. It is well known that an Arithmetic and Logical Unit is one of the most fundamental operational units in the quantum processor (ALU). The design and implementation of an innovative r/q 16-bit ALU that improves the overall performance of quantum processors while carrying out the task in the digital signal processing domain are discussed in this study. When reversible gates were used in place of logic gates, the power dissipation in terms of information bit loss was significantly reduced. Simulation of these circuits is done by QCA Designer tool and language used for programming is very high-speed hardware integrated circuit hardware descriptive language, Verilog HDL. The power and delay analysis of the various sub modules is performed and a comparison with the traditional circuits is also carried out. The designed ALU has better efficiency as it has less power loses and reduction in power loss upto 39 % is obtained.

Keywords: - Reversible logic gates, Fredkin Gate, Toffoli Gate, qALU, Low Power Dissipation, gates, QCA.

Introduction:

In present technology of the signal processing, the VLSI concept based on the power scattering is highly desirable because due of the increasing complexity of VLSI circuits, which grows every year as a result of the rising demand for more logical components in smaller volumes. As a result, power dispersion has emerged as the fundamental problem in the VLSI area. The fundamentals of reversible logic come from the thermodynamics of data preparation, as shown by typical irreversible logic circuits, which generate heat as a result of the loss of data during calculation. According to Landauer theory, heat is released from circuits built with irreversible components due to the loss of data bits. It is shown that losing one bit of data results in a loss of energy equal to KT*log2 joules, where K is the Boltzmann constant and T is the temperature at which the activity occurs. i.e., the conventional logic gates-based circuits with deuteriation in the performance of the processors. It is termed as reversible logic gate only if it has a dedicated output terminal for each input i.e., for a logical gate with n inputs there should be n outputs. Enhancing the capabilities of these logical circuits has been an important research field that must work at low power levels due to the growing desire for more portable, smaller system designs with greater

speeds. In addition to the power dissipation and energy consumption in the various modules of the ALU there are certain other parameters that effects the performance of the quantum processor such as delay in the signal propagation, packaging density, etc. Landauer has also submitted that with the use of the irreversible logic gates i.e., traditional one always leads to energy dissipation regardless of the development in the ongoing technology using the CMOS gates. As a result, one of the best solutions to this problem is the ability to express an irreversible logic gate in terms of a reversible gate. Such circuits can be synthesised using the least amount of energy possible due to the one-to-one mapping between input and output, which results in very low power dissipation. As a result, reversible designs are becoming increasingly important in disciplines such as nanotechnology, low power CMOS design, and other cutting-edge applications. Reversible logic design aims to reduce quantum cost, delay, supplementary inputs, and garbage outputs, among other factors. It is abundantly evident from this explanation that reversible logic is the cutting edge in low power technology and is hence being used for the construction of qALUs. The information once lost cannot be recovered in any way, as it has been noticed that the conventional logic circuits emit heat for every piece of information lost during the execution of any task by the qALU. The recovery of the information will be possible thanks to the logical circuit built utilising reversible logic gates, which will improve the qALU and quantum processor's overall performance. According to the Bennett theory, if the circuit is designed with reversible logic gates that computes the performance based on the concept of thermodynamics, which taught us the advantages of the reversible process over irreversible process, the heat dissipation due to information loss can be avoided. [1-10].

The discussion so far has shown that there have been significant advancements in the usage of reversible logic, enabling better quantum computer algorithms and plans for matching computer designs. It has received a lot of attention as a potential logic design approach for use in contemporary nanotechnology and quantum computing with no effect on physical entropy. The design of reversible logic gate structures and arithmetic units has received the most significant contributions in the literature, however most researchers haven't put much work into designing reversible ALUs. Regardless of the method employed to construct the gates, classic irreversible gates in binary logic circuits always result in energy loss. Any future CMOS will have an impossible heat removal problem due to the power dissipation, making it impossible to speed up CMOS devices at some point in the near future. The Landauer theorem states that, if we ignore the technological and material aspects of computer manufacturing, the energy consumption in computers is mostly caused by logical irreversible operations. The widely used AND gate, which has two inputs and one output, loses one bit for each piece of data that passes through it. There will be kT generated for every bit of information lost, where k is the Boltzmann’s constant and T is the absolute temperature. The generation of heat is inevitable on logic because of the uses of traditional logic gates in computer. energy. The key point of reversible computing is that the electric charge on the storage cell consisting of transistors is not permitted to flow away when the transistor is switched. Then it can be reused through reversible computing, which can decrease the energy consumption. When there is no loss of information bits, then the system is reversible. In VLSI circuits, it means that the circuits consisting of AND & OR gate, the bit information presented by charge can be saved when it is not used, which leads to the reversibility of the system. Therefore, reversible computing is an appealing solution in many emerging fields such as nanotechnology, as well as quantum and optical computing [11-15].

As an alternative to CMOS-VLSI, an approach called the quantum cellular automata (QCA) has been developed in 1993 so as to compute the performance of the processor with quantum dots. Unlike conventional computers in which information is transferred from one place to another by electrical current, QCA transfers information by means of propagating a polarization state from one cell to another cell. Hence improving the speed by reduction in area is the main area of research in VLSI system design. The heart of every computer is an

Arithmetic Logic Unit (ALU). This is the part of the computer which performs arithmetic operations on numbers, e.g., addition, subtraction, etc. In digital systems the combinational circuits perform these arithmetic operations. In present VLSI Technology, Power Consumption has become a very important factor for consideration. By using Reversible gates for designing the circuits with reduced power consumption when compared to conventional design-based circuits. Reversible Logic finds its own application in Quantum computing, Nanotechnology, optical computing, and computer graphics and low Power VLSI. As having more advantages with reversible logic in digital circuits. In modern VLSI system power dissipation is very high due to rapid switching of internal signals. The complexity of VLSI circuits increases with each year due to packing more and more logic elements into smaller volumes. Hence power dissipation has become the main area of concern in VLSI design. Reversible logic has its basics from thermodynamics of information processing. According to this, traditional irreversible circuits generate heat due to the loss of information during computation. In order to avoid this information loss, the conventional circuits are modelled using reversible logic. Landauer [1961] showed that the circuits designed using irreversible elements dissipate heat due to the loss of information bits. It is proved that the loss of one bit of information results in dissipation of KT*log2 joules of heat energy where K is the Boltzmann constant and T is the temperature at which the operation is performed. Bennett [1973] showed that this heat dissipation due to information loss can be avoided if the circuit is designed using reversible logic gates. A gate is considered to be reversible only if for each and every input there is a unique output assignment. Hence there is a one-to-one mapping between the input and output vectors. A reversible logic gate is an n –input, n- output device indicating that it has same number of inputs and outputs. A circuit that is built from reversible gates is known as reversible logic circuit [16-20].

The advancement of reversible logic technologies has helped in improving the performance of computer architectures.

Reversible logic is widely being considered as the potential logic design style for implementation in modern nanotechnology and quantum computing with minimal impact on physical entropy. Significant contributions have been made in the literature towards the design of reversible logic gate structures and arithmetic units. However, there are not many efforts directed towards the design of reversible ALUs. The Binary logic circuits built using traditional irreversible gates inevitably lead to energy dissipation, regardless of the technology used to realize the gates. The power dissipation in any future CMOS will lead to an impossible heat removal problem and thus the speeding-up of CMOS devices will be impossible at some point of time in near future. According to the theorem of Landauer, if we do not consider the factors of technology and material in the manufacture of computer, the energy consumption in computer is mainly produced by the logical irreversible operations. The commonly used gate- AND gate, which has two inputs and one output, one bit lost when the information bits go through this gate. For every bit of information loss, there will generate $kT \ln_2$ joules, where k is the Boltzmann's constant and T is the absolute temperature. The generation of heat is inevitable on logic because of the uses of traditional logic gates in computer. The loss of energy can be minimized or even prevented by applying the principle of reversibility to the operation of digital circuits. It can be shown that for power not to be dissipated, it is necessary to build a circuit from reversible gates. This solution based on the reversible logic promises a circuit operation with arbitrarily small fraction of signal energy. The key point of reversible computing is that the electric charge on the storage cell consisting of transistors is not permitted to flow away when the transistor is switched. Then it can be reused through reversible computing, which can decrease the energy consumption. When there is no loss of information bits, then the system is reversible. In VLSI circuits, it means that the circuits consisting of AND and OR gate, the bit information presented by charge can be saved when it is not used, which leads to the reversibility of the system. Therefore, reversible computing is an appealing solution in many emerging fields such as nanotechnology, as well as quantum and optical computing [21-25].

Reversible Logic Gates:

A circuit is said to be reversible if the input vector can be uniquely recovered from the output vector and there is a one-to-one correspondence between its input and output assignments, i.e., not only the outputs can be uniquely determined from the inputs, but also the inputs can be recovered from the outputs. Thus, the number of inputs and outputs in reversible gates are equal. Any arithmetic logic unit must be able to produce a variety of logic outputs based on inputs determined by the programmer for implementation in an instruction set architecture. Therefore, reversible logic devices used in an environment must have both fixed select input lines that receive opcode signals manipulated by the programmer and permanent output lines where the result of the logical output is produced. For an *n* input/output logic gate, if there is a one-to-one correspondence between its inputs and outputs, then this logic gate is reversible. That is to say, a reversible gate has the same number of inputs and outputs. Commonly used reversible gates are NOT gate, CNOT gate (Feyman gate), Toffoli gate, Fredkin gate and so on. In the design of reversible logic circuits, the following points must be considered to achieve an optimized circuit [26-27]. They are

- Fan-out is not permitted.
- Loops or feedbacks are not permitted.
- Garbage outputs must be minimum.
- Minimum delay.
- Minimum quantum cost.

Reversible gate is realized by using 1*1 NOT gates and 2*2 Reversible gates, such as V, V+ (V is square root of NOT gate and V+ is its Hermitian) and FG gate which is also known as CNOT gate. The V and V+ Quantum gates have the property given in the equations 1 to 3 [28].

$$V * V = NOT \quad (1)$$

$$V * V+ = V + * V = I \quad (2)$$

$$V + * V+ = NOT \quad (3)$$

The Quantum Cost of a Reversible gate is calculated by counting the number of V, V+ and CNOT gates.

NOT Gate

The Reversible 1*1 gate is NOT Gate with zero Quantum Cost is as shown in the Fig. 1.

Fig.1. Reversible NOT gate [29]

Feynman / CNOT Gate

The Reversible 2*2 gate with Quantum Cost of one having mapping input (A, B) to output (P = A, Q = A⊕B) is as shown in the Fig. 2.

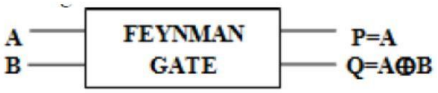

Fig.2. Reversible Feynman/CNOT gate (FG) [30]

Toffoli Gate

The Reversible 3*3 gate with three inputs and three outputs. The inputs (A, B, C) mapped to the outputs (P=A, Q=B, R=A.B^C) is as shown in the Fig.3. Toffoli gate is one of the most popular Reversible gates and has Quantum Cost of 5.

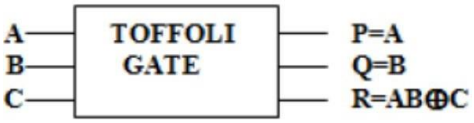

Fig.3. Reversible Toffoli gate (TG) [31]

n -Toffoli gate has *n* inputs and outputs, and the first (n-1) inputs are control bits, the input is targeting bit Fig. 4. It also can be called the Toffoli gate series.

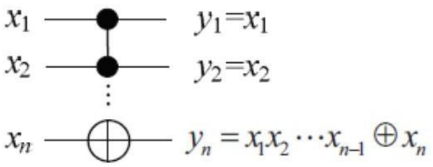

Fig.4. Reversible n-Toffoli gate (TG) [12]

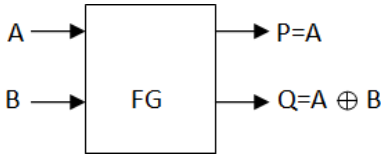

Fig.5. 2x2 Feynman gate [32]

Feynman gate is a 2×2 reversible gate as shown in below figure 5. The Feynman Gate is also called as CNOT gate i.e., controlled NOT gate. The Feynman gate is used to duplicate of the required outputs since Fan-out is not allowed in reversible logic gates. The Quantum Cost of FG is 1. This is also the primitive gate owing its importance in determining quantum cost metric.

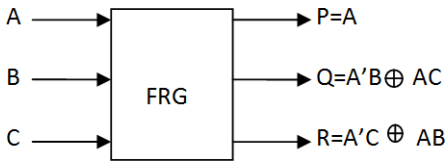

Fig.6. 3x3 Fredkin gate [33]

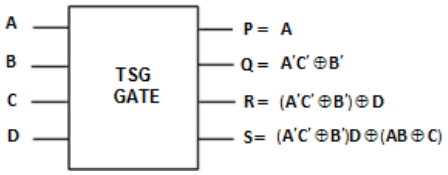

Fig.7.4x4 TSG gate [34]

The Toffoli Gate (TG) is a 3*3 reversible logic gate with three inputs and three outputs. The input to output mapping of a Toffoli gate can be represented as (A, B, C) to (P = A, Q = B, R = ((A B) ⊕ C), where A, B, C are the inputs and P, Q, R are the outputs of a Toffoli gate. Figure 7 shows the block diagram of a Toffoli gate. A Toffoli gate has a quantum cost of 5 as it can implemented using 2 V gates, 1 V + gate and 2 CNOT gates. Figure shown above gives the quantum implementation of a Toffoli gate [35].

In order to make a gate reversible additional input and output lines are added so that a one-to-one mapping exists between the input and output. This prevents the loss of information that is main cause of power dissipation in irreversible circuits. The input that is added to an m x n function to make it reversible is known as constant input (CI). Those outputs which are not used in the circuit is called as garbage output (GO). The number of garbage output for a particular reversible gate is not fixed. Several reversible gates have come out in the recent years. The most basic reversible gate is the Feynman gate which is a 2x2 reversible gate available and is commonly used for fan out purposes. The 3x3 reversible gates include Toffoli gate, Fredkin gate, all of which can be used to realize various Boolean functions. Fredkin gate. The 4x4 reversible gates include TSG gate, MKG gate, HNG gate, PFAG gate etc. shows the TSG gate. Some of the 4x4 gates are designed for implementing some important combinational functions in addition to the basic functions. The concept of reversible logic gates is used for reducing power consumption and loss of data. This logic uses the reversible gates which have same number of inputs and outputs. Some of the cost metrics like garbage outputs, number of gates, Quantum cost, constant outputs are used to estimate the performance of reversible circuits. A Reversible circuit design can be modelled as a Sequence of discrete time slices and depth is summation of total time slices. Various proposals are given to design of combinational and sequential circuits in the undergoing research. the design of different combinational circuits like binary comparator, Full adder, Full subtractor, Multiplexer circuits using Reversible Decoder is proposed with optimum Quantum cost. The design of different combinational circuits like binary comparator, Full adder, Full subtractor, Multiplexer circuits using Reversible Decoder is proposed with optimum Quantum cost [35].

Feynman/CNOT Gate

According to Figures 8 and 9, the Reversible 2*2 gate with a Quantum Cost of One maps inputs (A, B) to outputs (P = A, Q = A•" B). In this case, A controls the input, B regulates the input, and P and Q are the two outputs. Being a 2 x 2, the Feynman gate.

Toffoli Gate

The Toffoli Gate (TG) is a three-input, three-output reversible logic gate. A, B, and C are the inputs, and P, Q, and R are the outputs of a Toffoli gate, respectively. This is known as the input to output mapping of a Toffoli gate. A Toffoli gate's block diagram is shown in

Figure 10. Since two V gates, one V + gate, and two CNOT gates can be used to create a Toffoli gate, its quantum cost is 5. The quantum implementation of a Toffoli gate is shown in Figure 10.

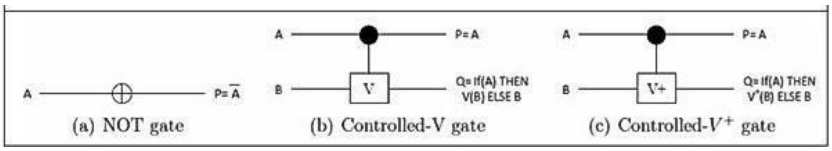

Fig.8. CNOT Gate implementation [35]

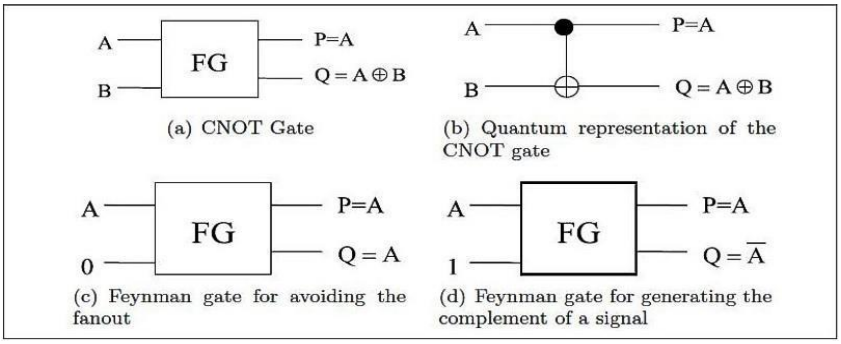

Fig.9.FG Gate Implementation [35]

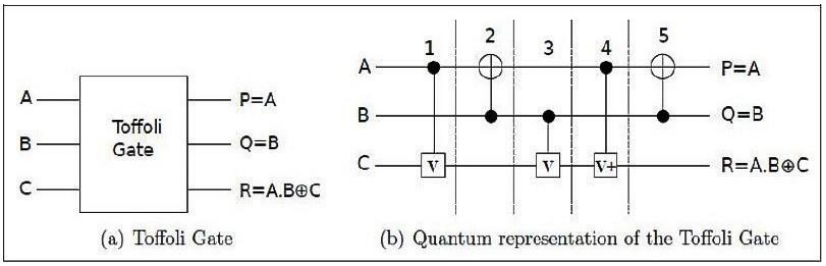

Fig.10.4x4 TG gate Implementation [35]

Peres Gate

It is a Peres gate, 3x3. The output vector is O, while the input vector is I (A, B, and C) (P, Q, R). P = A, Q = A B, and R = AB C define the output. A Peres gate has a quantum cost of 4. A 3*3 Peres gate is depicted in Figure 11.

Fredkin Gate

A 3*3 reversible logic gate called a Fredkin gate has three inputs and three outputs. A, B, and C are the inputs and P, Q, and R are the outputs, respectively, of the Fredkin gate, which transforms (A, B, and C) to (P = A, Q = A B + AC, and R = AB + A C). Given that it can switch its other two inputs based on the value of its first input, a Fredkin gate can function as a 2:1 MUX. A 2*2 Feynman gate with a quantum cost of 5 and two dotted rectangles is identical to a quantum cost of 1, 1 V, and 2 CNOT gates, as shown in Figure 12.

Double Peer Gate (DPG)

Two 3*3 Peres gates are cascaded to create a DPG gate. This gate has a quantum realisation cost of 6. because it has two 3x3 Peres gates. When the gate's fourth input is set to zero (D = 0), as shown in Figure 13, it can function alone as a reversible full adder circuit [36].

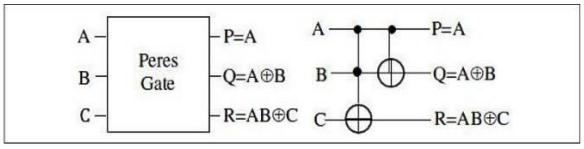

Fig.11.4x4 Peres Gate Implementation [36]

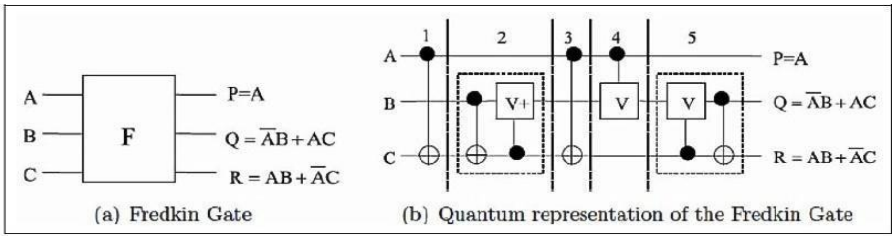

Fig.12.4x4 Fredkin Gate arrangement [37]

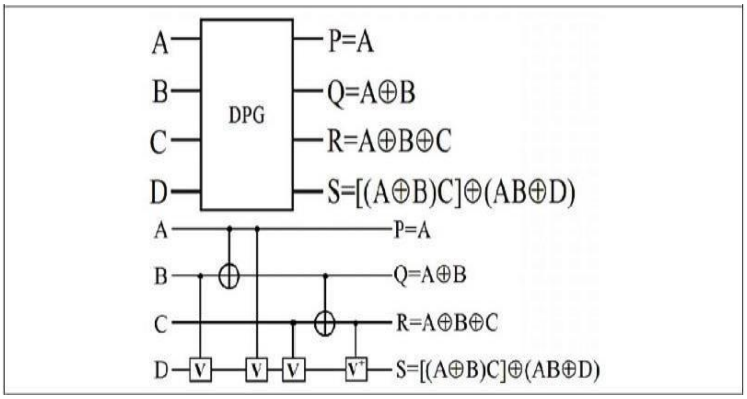

Fig.13.4x4 Double Peres Gate Implementation [38]

ALU Architecture

The fundamental arithmetic and logical operations are carried out by the Arithmetic Logic Unit (ALU). The arithmetic extender, logical extender, and multiplexer that make up the ALU are depicted in Fig. 14 below. The ALU's operation will be determined by the control signals. Moreover, there is a mode control input that lets you choose between logical and mathematical operations.

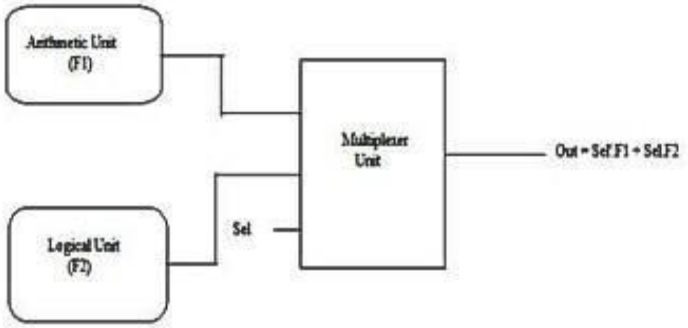

Fig.14.Block Diagram of ALU [39]

A crucial component of the CPU is the arithmetic and logic unit (ALU), which is a data processing unit. Although there are many different CPU types, every CPU has an ALU. The DM74LS181, a 4-bit ALU that can carry out all 16 possible logic operations on two variables as well as a number of arithmetic operations, serves as the proposed design's reference logic. ALU offers 16 arithmetic operations, including add, subtract, compare, and double in addition to the previous twelve operations. provides 16 two-variable logic operations, including EXOR, comparison, AND, NAND, OR, and NOR, in addition to ten more operations [40].

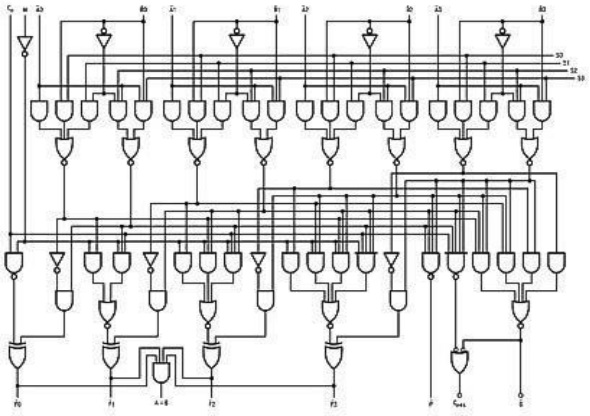

Fig. 15 Logic Diagram of conventional ALU [41-42]

The diagram below depicts the architectural layout upon which the 16-bit ALU is built.

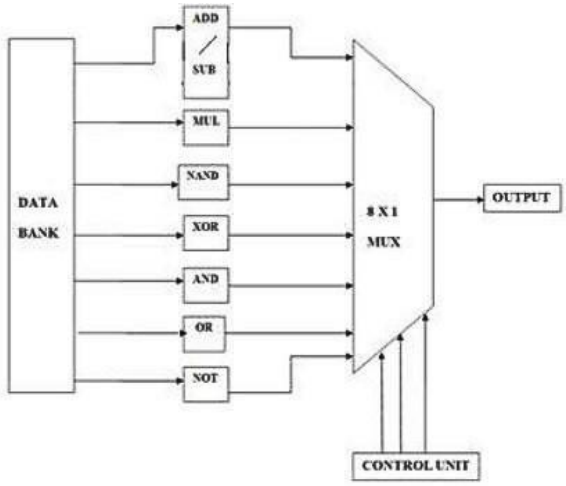

Fig. 16 Another ALU Architecture [43-44]

Proposed Design of qALU using Reversible Logic Gates:

This section presents the 16-bit ALU. Toffoli, Fredkin, Feyman, and DPG gates are used in the construction of the Arithmetic and Logical Units. The Proposed ALU performs four logical operations and eight arithmetic operations. The table of tasks assigned to the reversible ALU is shown in Table 1. This ALU is designed to minimise power losses while maintaining a low circuit cost. After performing these functions, the simulation of the ALU is carried out. The power analysis of the irreversible and reversible ALUs is then completed and compared.

Table 1. Functional Table for Reversible/ Quantum ALU (rALU/qALU)

S	S_0	S_1	C_{in}	Fun
Zero	Zero	Zero	Zero	Sum
Zero	Zero	Zero	One	Sum with Carry
Zero	Zero	One	Zero	1's compliment Sum
Zero	Zero	One	One	Subtraction
Zero	One	Zero	Zero	Delayed bit
Zero	One	Zero	One	Increment Accumulator
Zero	One	One	Zero	Decrement Accumulator
Zero	One	One	One	Accumulator value
One	Zero	Zero	x	XOR Operation
One	Zero	One	x	AND Operation
One	One	Zero	x	OR Operation
One	One	One	x	NOT Operation

The ALU is regarded as the system's brain in the processor architecture. A mathematical and logical unit ought to be able to produce a greater variety of feasible mathematical and logical operations. Reversible gates should optimise the operations of the arithmetic and logical unit in order to make the ALU design based on this structure possible. However, in order to reduce circuit delays, the cost of the circuit chooses the lines that are used to design the circuit. To do this, at each stage, it should be verified that every part of the design is reversible, and the outputs should propagate in a way that both ensures the circuit's proper operation and achieves reversibility. The arithmetic unit is in charge of managing the program's arithmetic operations. The new reversible gates serve as the foundation for the suggested arithmetic unit's construction.

Table 2. Functionality Table of qALU

Control Inputs			Output	Results
C0	C1	C2		
Zero	Zero	Zero	B Value	Transfer B
Zero	Zero	One	Increment B	Increment B
Zero	One	Zero	Sum	Addition
Zero	One	One	Sum with Carry	Addition with carry
One	Zero	Zero	Sum	1's complement subtraction
One	Zero	One	Sum with Carry	2's complement subtraction
One	One	Zero	Decrement B	Decrement B
One	One	One	B Value	Transfer B

Another crucial component of the central processing unit is the logical unit, which manages the logical operations carried out by the programmer. The new reversible gates serve as the foundation for the suggested logical unit design. Based on the equation below, the output function is realised.

$$F_1 = (AC_0 + AC_1) XOR\ B\ XOR\ C_2 \quad (4)$$

Where C0, C1, and C2 are the control inputs while A and B are the inputs to the reversible gates.

The following output equation can be used to design the functionalities of a logical unit:

$$F_2 = \bar{A}\bar{B}C_0 + A\bar{B}C_1 + \bar{A}BC_{2+}ABC_3 \quad (5)$$

The values of C0, C1, C2, and C3 are used as control inputs depending on the control input values, which can be generated by altering the inputs' 0:1 logical function combinations.

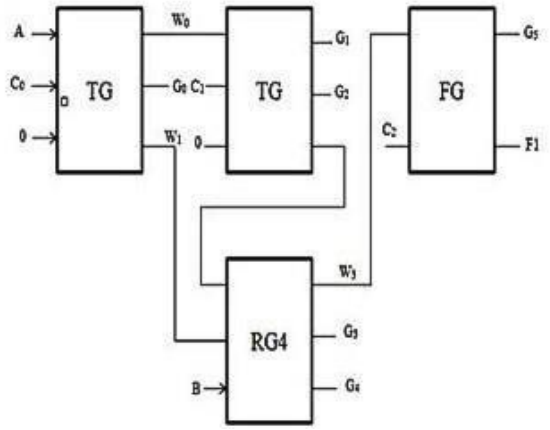

Fig. 17 qALU Design using TG, RG4 & FG Gates

The function generator's function is to process the Ai and Bi input data under the control of the S0, S1, S2, and S3 parameters, and then produce the combined functions Xi and Yi at the output side, where Xi is the combined function on Ai and Bi controlled by the S3 and S2 parameters and Yi is the combined function on Ai and Bi controlled by the S1 and S0 parameters.

$$X_i = \overline{S_3 A_i B_i} \; S_2 A_i \overline{B_i} \quad (6)$$

$$Y_i = \overline{S_1 A_i B_i} \; S_0 A_i \overline{B_i} \quad (7)$$

The reversible function generator is depicted in Figures 17, 18, and 19 together with its accompanying package diagram, which corresponds to the aforementioned logical statement.

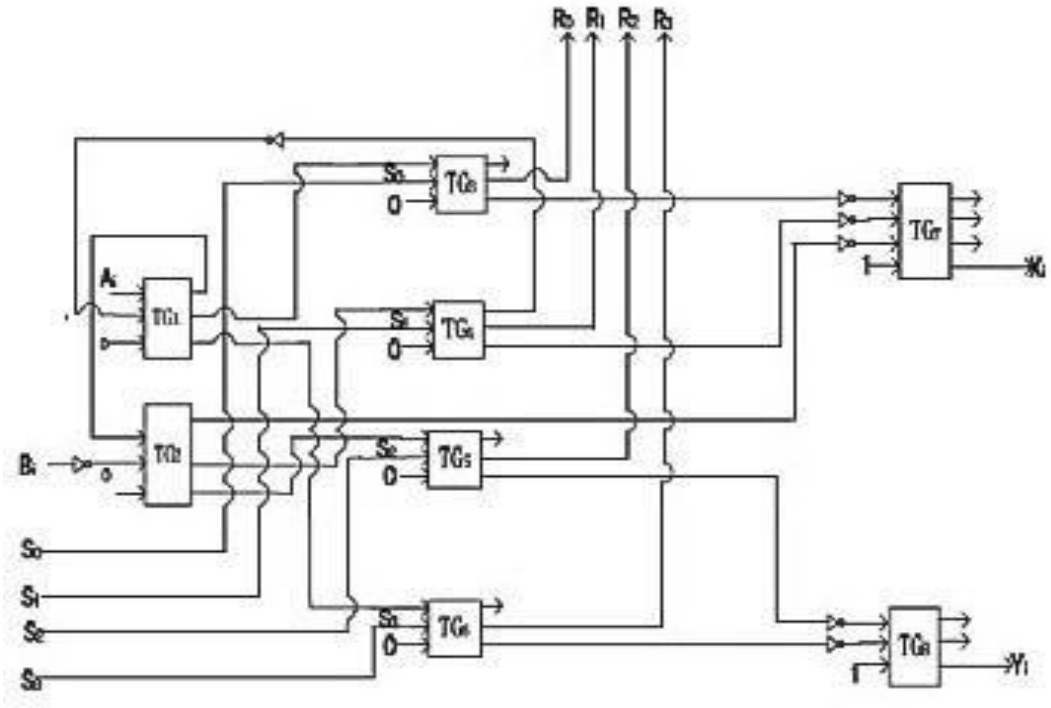

Fig. 18 The reversible function generator

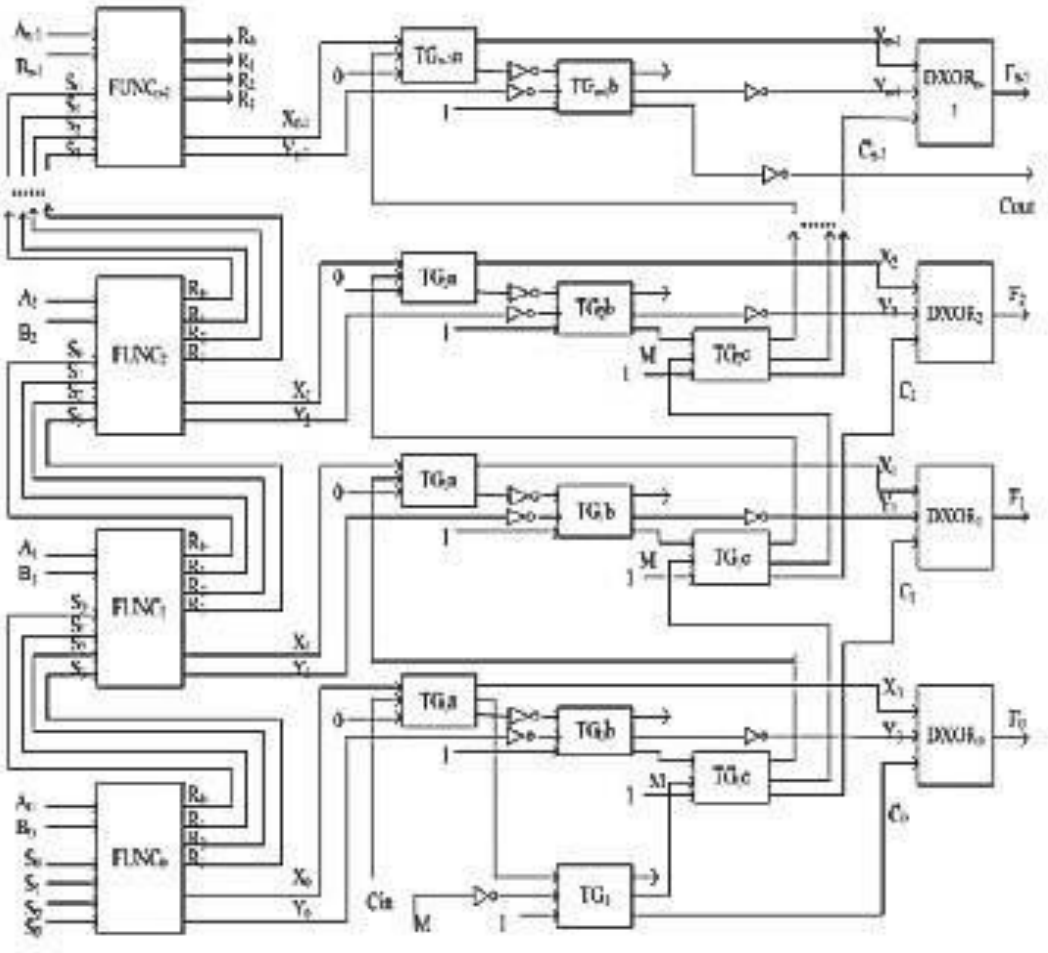

Fig. 19 The block diagram of Reversible ALU

Based on equations 5 to 7, the output signals Xi and Yi are produced after the input signals Ai, Bi, and S0 to S3 have passed through the reversible function generators Xi and Yi as the first and second input signals, respectively, of the reversible control unit DXORi. The third input signal Ci of the reversible control unit DXORi is then obtained by operating with the control signal M. By carrying both the select lines S0, S1 and carry output to the following stage, the single bit structure of the arithmetic unit is converted into a 16-bit purposed structure. The intended 16-bit arithmetic unit has 48 garbage outputs, 80 ancilla inputs, and so forth. Similar to 16-bit arithmetic units, N bit arithmetic units can be created and have 5N ancilla inputs and 3N trash outputs. By propagating the select lines S0 and S1, a 16-bit structure of the logic unit can be created from a single bit reversible purposed structure.

Ancilla inputs and trash outputs for this 16-bit logic unit will total 64 and 80, respectively. There will be 190 gates overall for 16 bits. Similar to a 16-bit logic unit, an N-bit logic unit can be created with 4N ancilla inputs, or constant inputs, and 5N trash outputs. number of gates overall 10 N gates.

Simulation Results & Discussion:

Our reversible Arithmetic and Logical Unit (qALU functional)'s validity is confirmed by simulating it using the ISE simulator. M, S0, and S1 are select lines, and A and B are two 16-bit inputs. The 16-bit output is enjoyable. The simulation of a 16-bit reversible Arithmetic and Logical Unit is shown in below Figures (qALU). Similar to pre-synthesis simulation, post-synthesis simulation is also carried out.

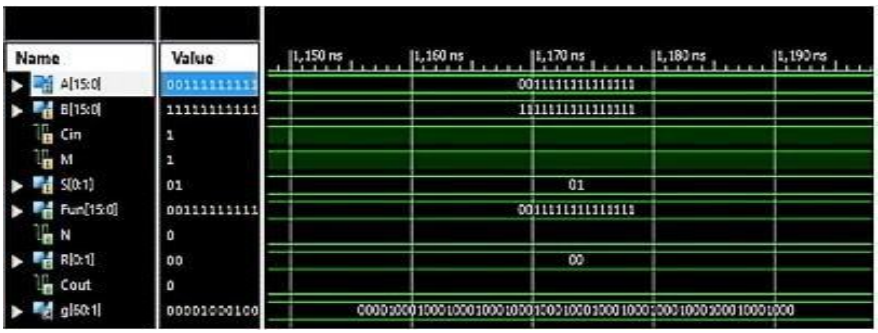

Fig. 20 Simulation waveforms of 16-bit Reversible Arithmetic and Logical Unit (ALU)

Power Analysis:

Each moment during the design cycle, the Xilinx Power Analyzer may do a power analysis. The number of times a certain signal changes throughout a clock period is referred to as the signal rate, which plays a vital role in the power computation. This must be provided by the designer in order to do an effective power calculation. Reversible logic structures, in particular miraculous decrease in logic power, reduce the dynamic power usage. The following are some crucial power factors to take into account:

• Standby (static) power

The amount of power used by a gadget when it is turned on but not actively performing any function is known as static power (i.e., the device is not clocked).

• Active or dynamic power

Dynamic power is the quantity of energy a device uses when it is in use (i.e., the device is clocked). The 16-bit reversible Arithmetic Logical Unit's (ALU) total power is made up of both leakage power and dynamic power from the device. The total of input/output power, logic power, and data power, as depicted in Fig. 11, is known as dynamic power. Compared to irreversible arithmetic logical unit, it is lowered by 5.12%. (ALU).

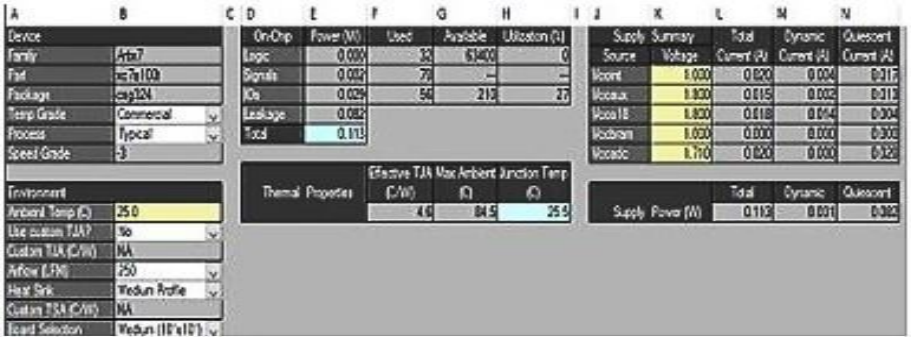

Fig. 21 Power dissipation for 16-bit reversible Arithmetic and Logical Unit (ALU)

• Power input/output

When the device is configured but there is no switching action, this is the power dissipation. The 16-bit reversible Arithmetic and Logical Unit (ALU) has an input/output power of 28.86 mW, whereas the 16-bit irreversible ALU has an input/output power of 37 mW.

• Data Strength

Data switching is what causes data power dissipation. Comparing it to a 16-bit irreversible Arithmetic and Logical Unit (ALU) that performs the same job, it is reduced using reversible logic gates by 34.78%. The 6-bit reversible Arithmetic and Logical Unit (ALU) has a data power of 1.5 mW.

• Power Logic

Logic power, also known as design dynamic power, is the additional energy used by user logic utilisation and switching activity. Reversible logic gates magically consume less power than traditional logic gates because their one-to-one input and output mapping prevents

bit loss. According to Table 3, a 16-bit reversible Arithmetic and Logical Unit (ALU) uses 53.3% less logic power.

Table 3. Power consumption-based Analysis

Source of Power	16-bit Irreversible ALU (mW)	16-bit Reversible ALU (mW)
Logic Power	0.76	0.36
Data Power	2.5	1.6
I/O Power	39	27.5
Total Power	40.08	30.52

Power dissipation comparison for 16 bits Arithmetic and Logical Unit (ALU)

- **Area comparison for Arithmetic and Logical Unit (ALU)**

Table -4 shows the area comparison between irreversible and reversible Arithmetic and Logical Unit (ALU). The Area is reduced by 33.33% by using reversible Arithmetic and Logical Unit.

Table 4. Area Comparison of 16-bit ALU

Parameters	16-bit Irreversible ALU	16-bit Reversible ALU
No of Slice LUTs	49	31
No of Occupied Slices	24	18
No of LUT Flip Flops pair Used	49	30

Verilog HDL is used to design each and every component of the reversible ALU (structural form of coding). Using the modelsim simulator, mentor visuals are used to emulate Verilog code. Variables are used to represent the input and output signals, and Toffoli gate modules are used to package a variety of Toffoli gates so that they may be instantiated as objects. The simulated outcomes have been submitted in below figures.

The simulation work of the proposed circuits has been carried out by using the QCA Designer tool for the most important and effective parameters of the module of the qALU such as Delay, packaging density, Number of cells, Garbage in, Garbage out etc. These are the parameter which are used to analyse the performance of the qALU with the use of the reversible logic gates, primarily Toffoli and its combination.

In addition, this this performance evaluation, power dissipation and the energy used to execute the task by the processor has been also carried out by using different available tools such as VHDL, Xilinx, MATLAB, etc. The figures from 20 to 38 have been put forward for the performance analysis of the qALU of the quantum processor that has got tremendous application in the field of DSP, Quantum Computation, Space data computation, Military data analysis, etc.

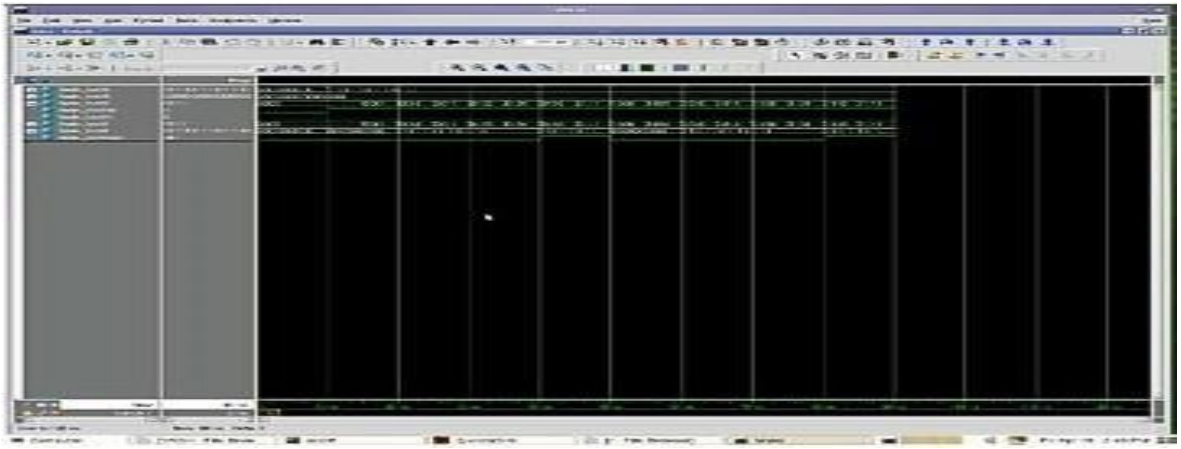

Fig. 22 Waveform of Arithmetic operation of reversible ALU

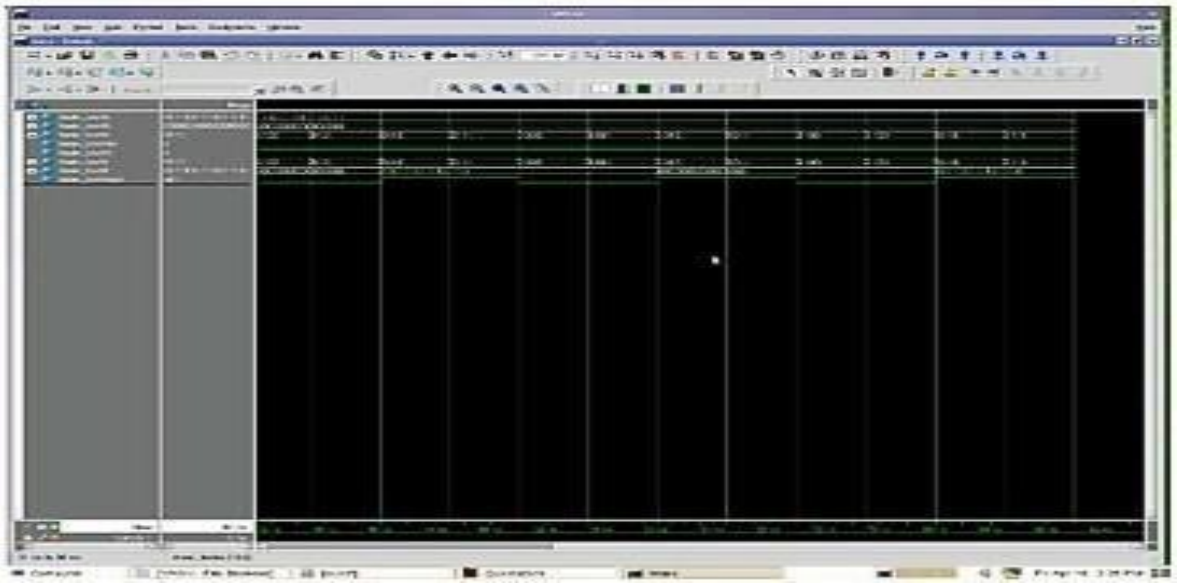

Fig. 23 Waveform of Logical operation of reversible ALU

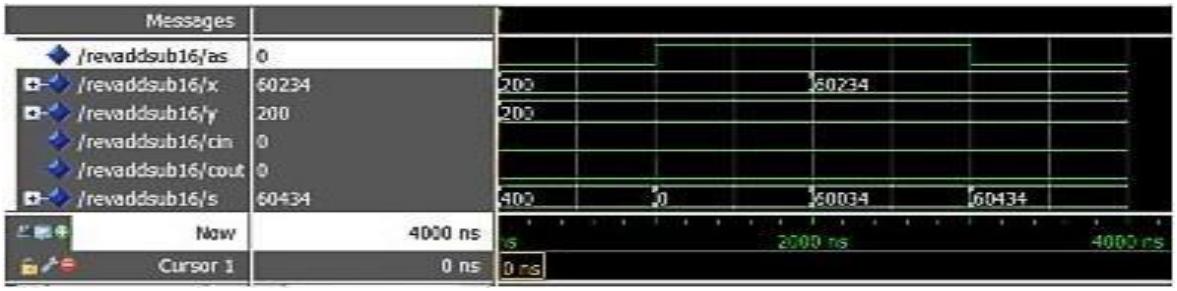

Fig. 24 Reversible 16bit adder/subtractor

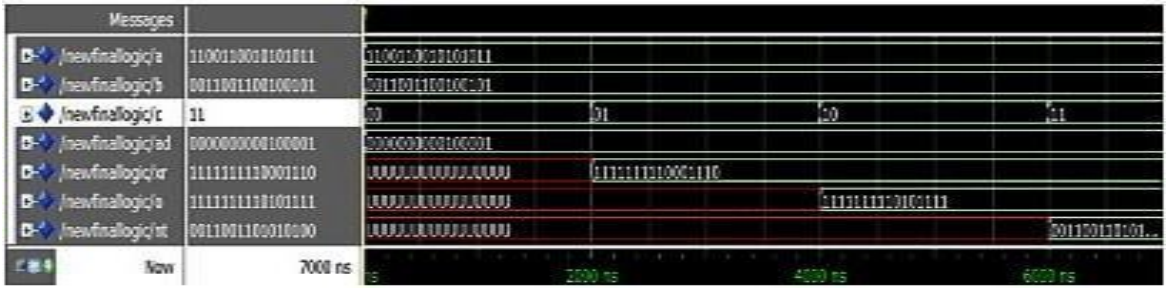

Fig. 25 Reversible 16-bit logical unit

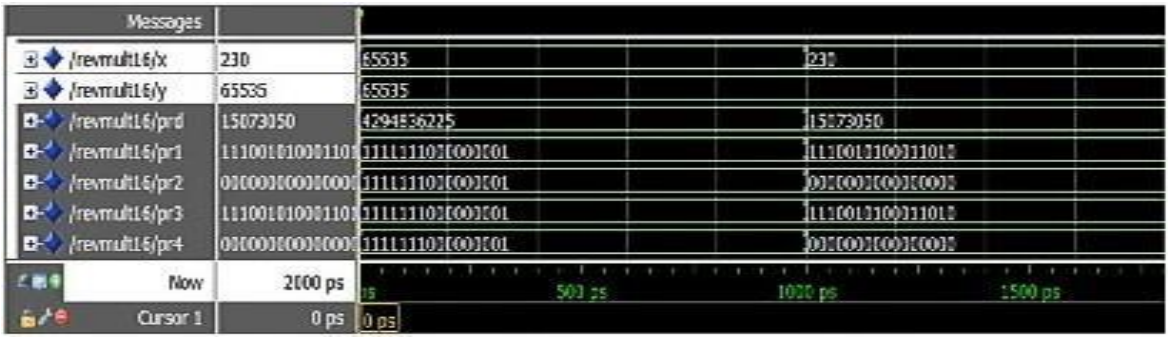

Fig. 26 Reversible 16 x 16 multiplier

Fig. 27 AU Design and simulation result

Fig. 28 LU Design and Simulation Result

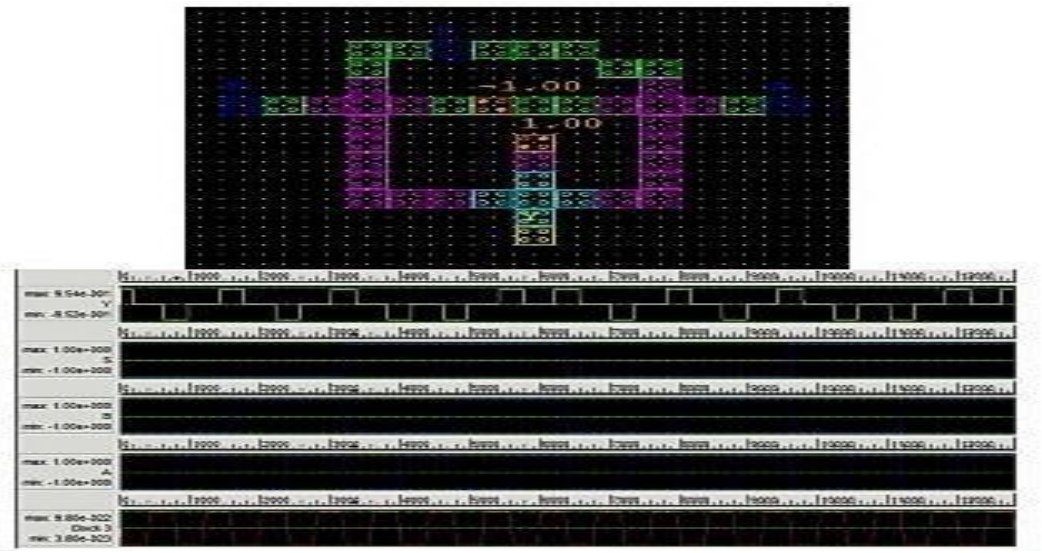

Fig. 29 Multiplexer design and simulation result

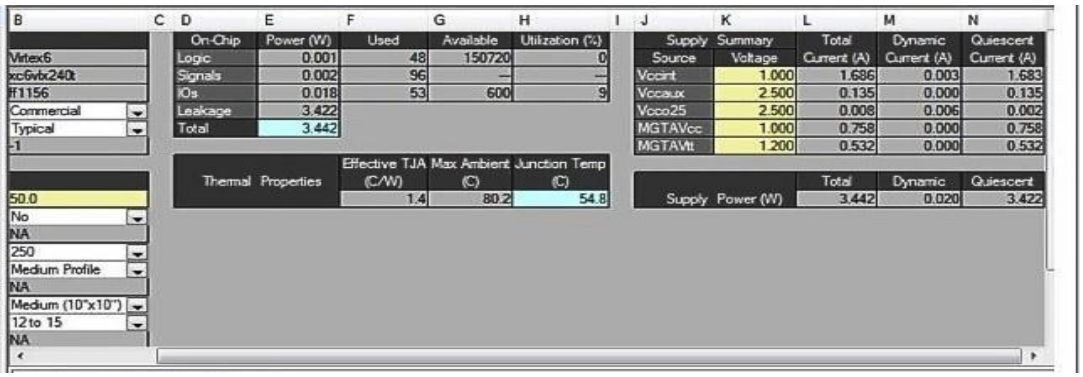

Fig. 30 Total Power for 16-bit Traditional ALU

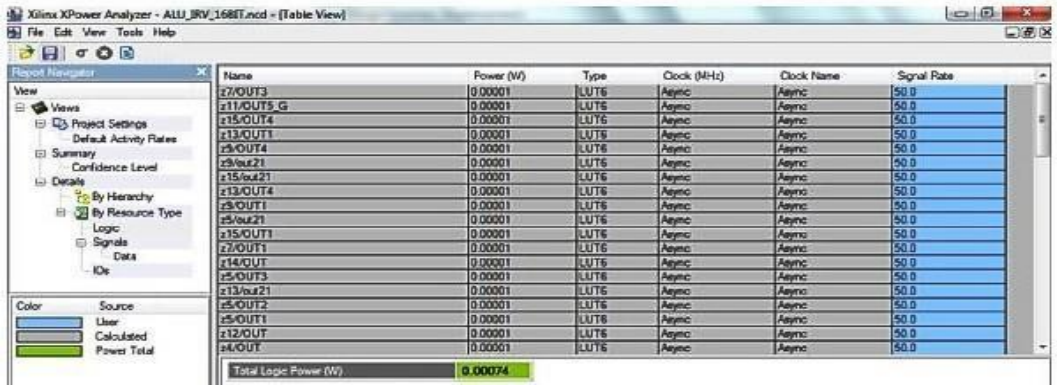

Fig. 31 Logic Power for 16-bit Traditional ALU

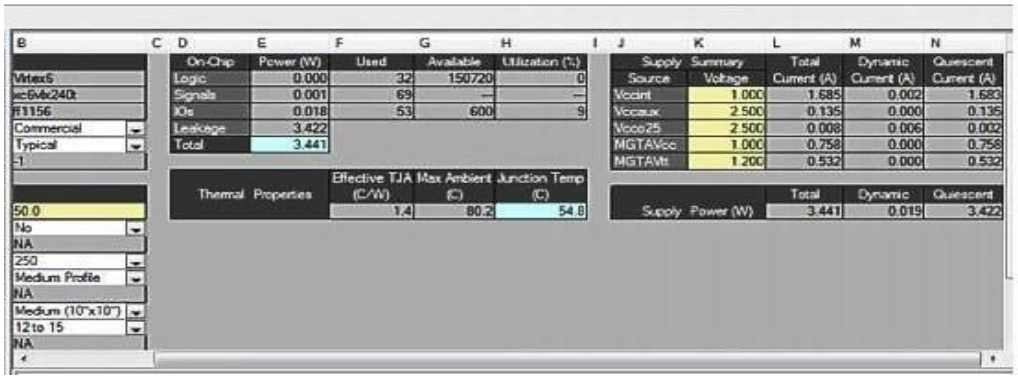

Fig. 32 Total Power for 16-bit Reversible qALU

Fig. 33 Logic Power for 16-bit Reversible qALU

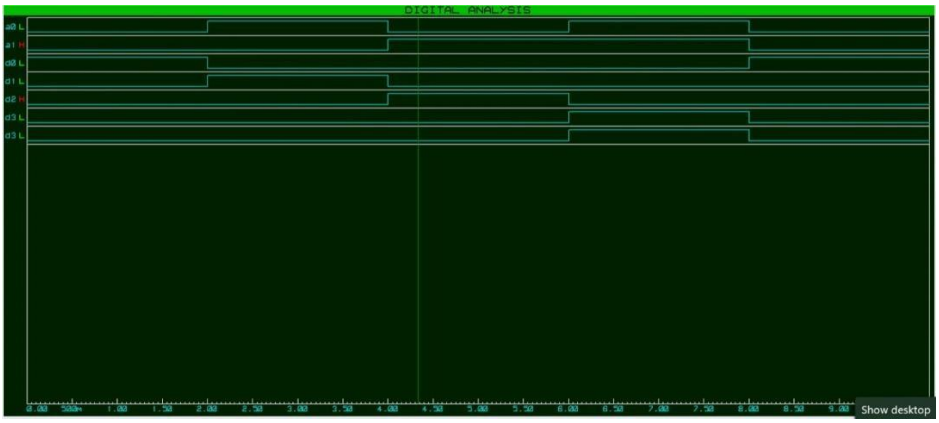

Fig. 34 Analysis of Decoder Circuit

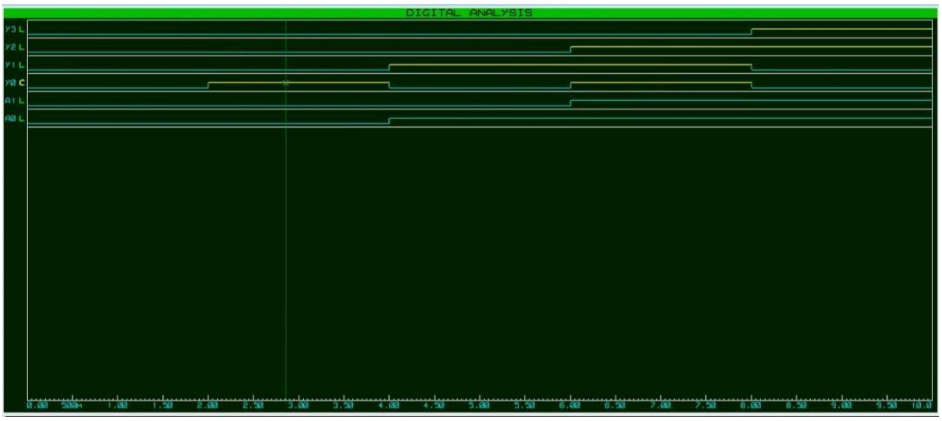

Fig. 35 Analysis of Encoder Circuit

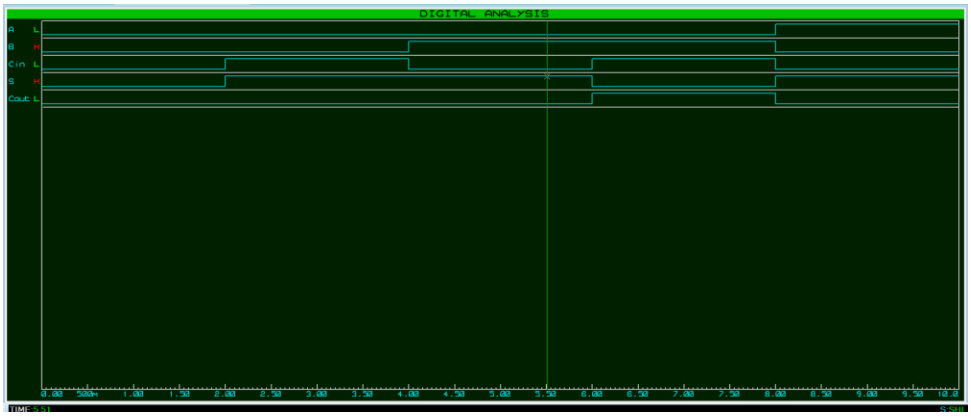

Fig. 36 Analysis of Full Adder Circuit

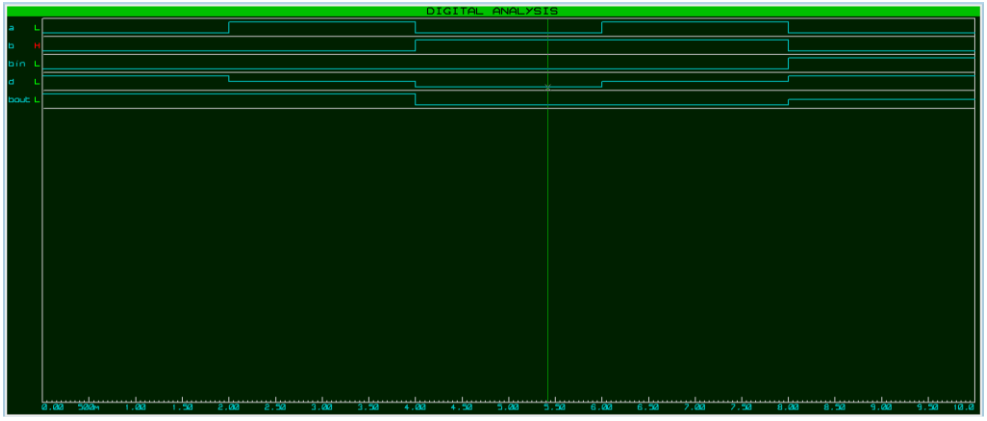

Fig. 37 Analysis of Full Subtractor Circuit

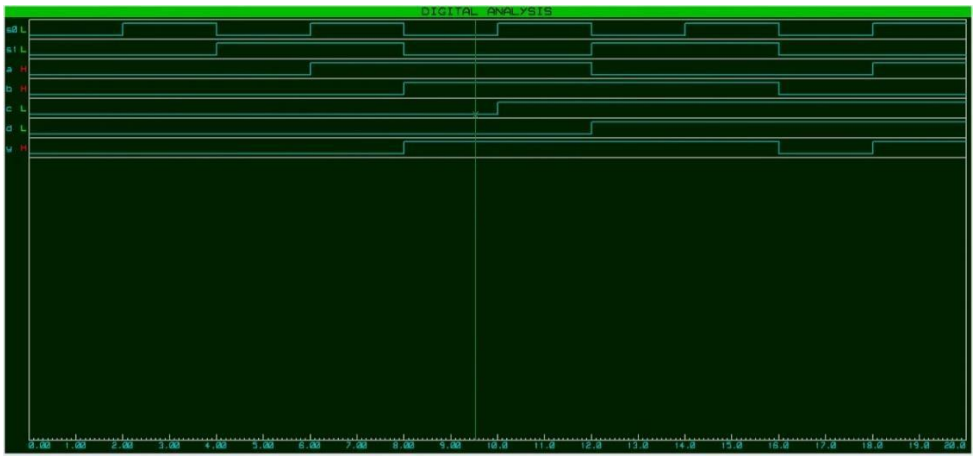

Fig. 38 Analysis of MUX Circuit

Conclusion:

Using Toffoli reversible logic gates, we have suggested the design and implementation of a 16-bit reversible ALU. Reversibility greatly lowers information bit use and loss, resulting in optimal power consumption. Mentor graphics simulation is used to test the performance of various components. The topic of discussion has been logical reversibility, or the ability of inputs and outputs to be separately retrieved from one another. The key question is if we can create physical gates and circuits that can genuinely run backward and expend almost no power. In the future, physical reversibility can also be analysed. In comparison to irreversible ALUs, the new reversible ALU designs favour low power dissipation and also occupy less space, both of which are desirable for the construction of a reversible central processing unit. Verilog HDL is used for RTL coding, and ISE Simulator is used for simulation. Xilinx 14.7 is used for synthesis. Using XPower analyzers, it is predicted that the power is decreased by 53.3% and the area is reduced by 33.33% for the logic, respectively. The research's findings have significant applications in low power and quantum computing. The potential application of Moore's law via quantum computing with reversible logic during the next few decades is covered under the research's future scope. Applications for this reversible Arithmetic and Logical Unit (ALU) include low power VLSI designs, optical computing, nanotechnology, quantum computing, and others. Complex logic architectures will benefit more from the extended operations. By utilising the proposed reversible Arithmetic and Logical Unit (ALU) design, numerous ASICs-based projects may be feasible. Comparing the proposed qALU to the existing reversible gates, which predominantly use the Reversible Arithmetic and Logic Unit (qALU), which is validated in the QCA platform, reveals an improvement in terms of optimization parameters for reversible logic. The proposed 16 bit reversible arithmetic and logic unit exhibits a remarkable improvement in the simulation restrictions, such as area, simulation time, and number of design-used cells, as well as the reversible logic design parameters. Because of this, the suggested system has a small footprint with QCA and less power loss with reversible logic.

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