A Review of Frequency Compensation Technique In Multistage Operational Amplifier For Low Power &High Gain Applications

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Abstract
Operational transconductance amplifiers (OTAs), are the rudimentary components for many analog systems, have received a loads of enthrallment in the literature due to their three-stage compensation. Over the recent years, a wide range of conclusions to the stability issue of such OTAs have been put forth, each with a idiosyncratic set of attributions or intended use. This study catechizes a wide range of anteriorly prevalent designs, insinuates a novel genus system that illuminates traits that unfold to be ubiquitous to various compensation structures, and enlighten which kind of OTA is best for a given application.

Keywords—three-stage, Miller compensation technique, nested Miller compensation technique, reverse nested Miller Compensation technique, wide load range, Low power, Frequency Compensation, Performance Boosting.

Introduction

In the contemporary period, all hardware devices have avant-garde, and all the breakthroughs is immigrating from the analog to the digital preserve, whilst for every digital circuit, analog circuits is still the foundation and there are countless researchers working in the analog and mixed fields, and they are more impassioned with this aspect[1-4]. Op-amps are vital constituent of all analog and mixed circuits and perform a pivotal role in these realms. [5] & [6]. For the best rendition of Op-amps, the VLSI industry is most indulged with reducing space, power consumption, settling time, slew rate, UGBW, and DC gain[7].These are direct connected high gain amplifiers with the capability to amplify small signals with virtually zero dimensionality. Differential amplifiers are recognized as single stage Op-amps, and as a result, their gain is minimal. A gain stage can as in cure to this problem by improving DC gain and dispensing an incentive for amplification. The level shifter is the next stage, and its primary function is to lower the DC level such that it is near the ground, which is made possible by the unbalanced output stage. The primary intend of an emitter follower is to deliver DC isolation in between the input & output for lessen the effects of loading. Cascading causes a loading effect. Two separate input terminals inverting and non-inverting and one output terminal are present in an amplifier's operation. [8]. Designers faced numerous trade-offs while attempting to develop an operational amplifier, as they grappled with a multitude of issues. The critical performance parameters of operational amplifiers (op-amps) are slew rate, input impedance, output impedance, frequency range, open loop gain, offset voltage, common mode rejection ratio, power supply rejection ratio, phase margin, and settling time. Operational amplifiers come in a variety of types relying on their intended use. Analogous to single-stage, two-stage, three stage, foldable operational amplifier, and telescopic operational amplifiers, differential amplifiers are witnessed as single stage operation amplifiers since their first stage is a differential amplifier with differential input and output [9]. The increasing speed and reduced power consumption of digital circuits can be attributed to the continuous and aggressive scaling down of CMOS technologies. Nevertheless, the acquisition of these privileges is accompanied by a trade-off in the form of reduced intrinsic device gain, hence compromising the efficiency of analog circuits [10]. Conversely, operational transconductance amplifiers (OTAs) with larger DC gain are necessary for high-precision applications. Transistors have conventionally been stacked upright in a cascode design to unravel this issue and garner high DC gain with virtually first-order response. But in precedence to testify device reliability, supply voltages must likewise be dialed back as scaling progresses. Because of this, there is less signal headroom, which makes traditional cascode approaches erratic. [11,12]. For this reason, modern OTAs gravitate to perform a cascading of multiple stages to excel the coveted gain. Even though many authors have substantiated the propitious design of four-stage OTAs [13-15] and many have gone over for describing n-stage OTAs [12–14 16-18], three-stage OTAs have drew a lot of research stake for a multifariousness of employments because they prevail to trot out a good trade-off between intricacy and power efficacy. Applications for three-stage OTAs comprise capacitive MEMS sensors, low-dropout (LDO) linear regulators, LCD drivers, and headphone amplifiers. [11,19-22]. For some applications, the amplifier needs to be able to deliver a very wide range of load capacitance that span multiple

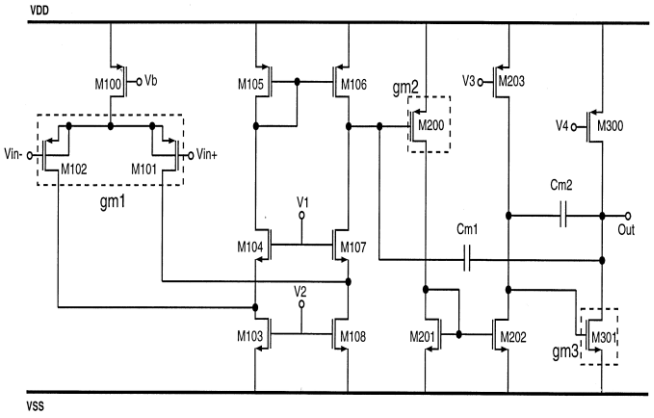
orders of magnitude. For other applications, the amplifier needs to be able to drive very high capacitive loads. [11,23-24]. The compensation of the consequent three-pole system is the primary asperity in three-stage OTA design. Numerous scholarly endeavors have been dedicated to the pursuit of formulating intuitive mathematical representations for the transfer functions of three-stage operational transconductance amplifiers (OTAs). Once the compensation structure is provided, the complexity of the advanced compensation designs designed to tackle this problem makes it difficult to conduct a manageable and intuitive analysis. [25-29]. These works enable engineers to easily extract pole and zero frequency expressions for use in manual analysis and design, but they make no verdict regarding the relative privileges of various compensation schemes.

Compensation Techniques used to Optimize the Performance of Operational Amplifiers

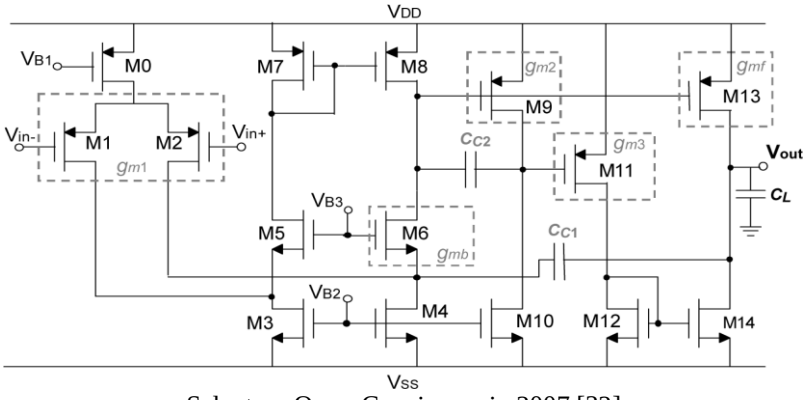
In 2001 Ka Nang Leung and Philip K. T. Mok stipulated novel stability necessity for low-power CMOS nested Miller compensated amplifiers. Then, a better rendition is developed that combines the benefits of a nulling resistor with a feed forward transconductance stage. The frequency responsiveness, transient response, and power supply rejection ratio are all improved by the proposed structure, according to experimental findings, without increasing power consumption or circuit complexity [34]. An active-feedback frequency-compensation (AFFC) technique for low-power operational amplifiers is depicted by Hoi Lee in 2003.The AFFC amplifier utilizes an active-feedback mechanism to effectively separate the low-frequency high-gain path and high-frequency signal path. This separation allows for the simultaneous achievement of high gain and wide bandwidth in the amplifier. The active-feedback network's gain stage additionally decreases the dimensions of the compensation capacitors, resulting in the reduction in overall chip area of the amplifier and an enhancement in the slew rate. In addition, the inclusion of left-half-plane zero inside the proposed AFFC topology enhances the stability & settling characteristics of the amplifier. An HGB and an HSB, respectively, divide the low-frequency and high-frequency signal channels in the active capacitive feedback network. The HSB greatly increases the amplifier's bandwidth while the HGB offers a high dc gain since it bypasses the intermediate high-gain stages with slow responses at high frequencies. The AFFC amplifier may thus simultaneously attain high gain and wide bandwidth. Because smaller compensation capacitors are needed, the chip size of the AFFC amplifier is likewise lowered. Furthermore, the presence of LHP zero in the amplifier enhances both stability and transient responses. The suggested AFFC amplifier outperforms other published compensation topologies in both small and big signal applications furthermore lacking a distinct feedback path [45]. Xiaohong Peng and Willy Sansen presented the AC Boosting Compensation (ACBC) scheme in 2004which was a revolutionary frequency compensation method that uses less power. The internal step of the add an ac route compared to a traditional multistage amplifier, which increases slew rate, gain-bandwidth product, and other performance metrics without increasing overall power consumption. Analysis demonstrates that stability can be fully guaranteed [43].In their 2005 study, Feng Zhu and Shouli Yan introduced two novel approaches for lower-voltage three-stage amplifiers, namely the Nested Feed forward RNMC (NFRNMC) and Crossed Feed forward RNMC (CFRNMC). These approaches involve reversed nested Miller Compensation (RNMC) and are proposed as innovative methods in this research. Both approaches utilize double feed forward channels in order to eliminate the right-half-plane zero. In order to increase the phase margin, the second architecture introduces a left-half-plane zero. Two three-stage amplifiers are constructed utilizing the proposed methodology in order to demonstrate the advantages of the novel Reduced Noise and Mismatch Compensation (RNMC) techniques over the conventional RNMC architecture. Based on simulation data, it has been observed that the NFRNMC and CFRNMC amplifiers provide superior stability compared to conventional RNMC amplifiers, although having an equivalent gain-bandwidth product. The suggested AFFC amplifier outperforms other published compensation topologies in both small and big signal applications further more lacking a distinct feedback path[46].Alfio Dario Grasso in 2006 presented a three-stage operational transconductance amplifier (OTA) that can drive highly capacitive loads is designed using a straightforward compensation technique that solely uses passive components. The new solution uses two more resistors in comparison to the traditional nested Miller compensation technique, which allows for a roughly one-order-of-magnitude reduction in the values of the compensation capacitors[30].The reversed nested Miller compensation with nulling resistor (RNMCNR) and the reversed active feedback frequency compensation (RAFFC) are two frequency compensation methods that are used for three-stage operational transconductance amplifiers presented by Alfio Dario Grasso in 2007. The methods, which are based on the fundamental RNMC, exhibit a built-in advantage over conventional compensatory systems, particularly for large capacitive loads. Additionally, they are accomplished without the need for additional transistors, reducing the complexity of the circuit and the amount of power used. For each solution, a clear design process is created that uses phase margin as the primary design parameter[32]. In 2007 Cannizzaro presents design methods for nested-Miller frequency compensated three-stage CMOS operational transconductance amplifiers. The basic technique for a Class-A topology is first described, and then various adjustments are given for a Class-AB solution to boost swing, slew rate, and current drive capability. The methods created are straightforward since they don't impose unneeded circuit limitations and produce precise results. They can therefore be easily included into an analog knowledge-based computer-aided design tool, but they are best suited for a pencil and paper design [36]. A three-stage amplifier with a wide operating range (1 to 15 nF) has been introduced by Zushuyan in 2013. In terms of topology selection pole-zero placements, parameter sizing, and CL variability assessment, the used LFL analysis is significantly more insightful than conventional direct circuit analysis. CBMC + parasitic-pole cancellation is the ideal frequency compensation strategy. A wideband current buffer and an active LHP zero circuit significantly improve its transistor-

level implementation. Comprehensive circuit studies are performed, including those of differential-mode, common-mode feedback, noise, slew rate, and input/output range. On the basis of these assessments, a manual design technique and an optimization based on genetic algorithms are provided [38]. S. Mehdi Hosseini Largani and team in 2014, a brand-new single Miller capacitor for three-stage amplifier frequency compensation is suggested. The compensation block of a typical three-stage amplifier is formed by a differential stage, whose negative and positive inputs are coupled through a cascade capacitor to the third stage's input and output nodes. Analysis reveals that this configuration, with only a very tiny amount of compensating capacitor, considerably enhances the frequency domain performances of the entire circuit, including phase margin and gain-bandwidth product [44].Again in 2015Grassoand team described a design process for three stage CMOS that operates in the subthreshold range. The process focuses on creating ultra-low-power amplifiers that have a small silicon footprint yet can drive large capacitive loads. This work described a three-stage, ultra-low-power, subthreshold OTA and the associated design approach. To improve large signal performance, the OTA makes use of a class AB O/P stage with an extra slew rate enhancement circuit [33].In 2015, Sajad Golabi introduced a class AB operational transconductance amplifier consisting of three stages, characterized by a substantial slew rate. The utilization of the reversed nested Miller compensation technique is employed to stabilize the suggested operational transconductance amplifier (OTA). This allows for the improvement of the slew rate, which is accomplished by the implementation of class AB input and output stages. The utilization of flipped-voltage follower cells in the initial stage, together with switched capacitor level shifter in the subsequent stages, is employed to achieve the class AB operation[40]. Elena Cabrera-Bernal suggested a bulk driven operational transconductance amplifiers (OTAs) in 2016, straight forward high-performance architecture is provided. The three gain stages in the solution give intrinsic class-AB behavior with precise and reliable standby current regulation, overall good large signal &small signal performances are attained, which puts solutions far ahead of the competition in terms of technological advancement [41]. A three-stage, low-power, area-efficient CMOS operational transconductance amplifier (OTA) designed for very large capacitive loads C_L, is presented by A.D. Grasso in 2017. The frequency compensation network is implemented using a single Miller capacitor and an incorporated inverting current buffer. The transient response for large-signal is additionally enhanced by the use of feed-forward path & a slew rate enhancer. According to a thorough investigation of tiny signals, the proposed method does not show a drivable C_L upper limit. In order to achieve frequency compensation, the suggested technique makes use of a single-Miller capacitor and incorporated inverting current buffer in the first (folded-cascode) stage. The amplifier has highly compact circuit layout because to the use of straightforward common source configurations for specially the second & third stages. Small-signal analysis shows that, OTA behaves as a single-stage OTA for capacitive load greater than the minimum value. Additionally, a push-pull output configuration and a class-B slew rate enhancer circuit augmented the transient response [35].A performance-boosting frequency-compensation technique, feed-forward Gm-stage& regular Miller plus indirect compensation (FGRMIC), is demonstrated by Shubin Liu, Zhangming Zhu and team in 2018. The proposed structure consist of three parts that basically ensures stability& significantly improving the performance, such as gain bandwidth product, slew rate& sensitivity. The initial section comprises a feed forward transconductance stage, whereas the subsequent section consists of a Miller capacitor connected in series with a single resistor. The third component consists of a resistor in conjunction with an indirect compensation capacitor. This paper represents a comprehensive theoretical analysis and design considerations to illustrate the stability of the compensation scheme[42]. Sadegh Biabanifard in 2018 describes a novel and straightforward (RNMC) structure-based frequency compensation method for three-stage amplifiers. The circuit complexity and die area were decreased by using a single, tiny compensation capacitor, which also outperformed RNMC in terms of performance due to the cancellation of the second dominant pole by a zero, the suggested technique is also unconditionally stable [37].In 2018, Sadegh Biabanifard offered a comprehensive approach to the design of frequency-compensating multistage amplifiers. Various stage cases have been considered, including differential voltage and current blocks, as well as generic compensation blocks for both voltage and current states. The configurations have been elucidated via a matrix representation. The utilization of binary matrices was employed in the strategic approach to emulate amplifiers through the implementation of feedback networks. Evolutionary algorithms were employed to minimize symbolic transfer functions and determine optimal numerical values. Also, the ideal MOSFET DC bias conditions and dimensions were determined using a diagram-based design. It is important to acknowledge that the utilization of reduced transfer functions, as opposed to numerical methods, offers a more comprehensive comprehension of circuit design by symbolically determining the poles and zeroes [39].In 2019, Qi Cheng introduced a novel frequency correction technique for three-stage amplifiers that are responsible for driving capacitive loads ranging from picofarads to nanofarads. The cascode Miller compensation technique effectively extends the frequency response of the non-dominant complex pole. Additionally, the compensation capacitors are decreased in size using this approach. To address the issue of significant variations in the loading capacitance CL, an adaptive approach is employed to change the Q-factor. This is achieved by using a local Q-factor control loop. The Q-factor of the complex pole pair is a crucial parameter that influences both the frequency peak in the gain plot & the settling time of the suggested amplifier in the closed-loop step response. This Q-factor is regulated by the LQC loop, which additionally determines the appropriate amount of damping current to be injected into the associated parasitic node. In addition, a feed-forward transconductance stage is incorporated in parallel to enhance the slew rate, while a left-half-plane zero is introduced to augment the phase margin. [47].In a study conducted by Mehdi Zaherfekr in 2019, a novel modified strategy was introduced with the aim of improving the frequency compensation for three stage operational trans-conductance amplifiers. In the architecture of the new frequency compensation, the elimination of the right-half plane zero results in the removal of the common node of Miller compensation capacitors, commonly known as the feed forward path.

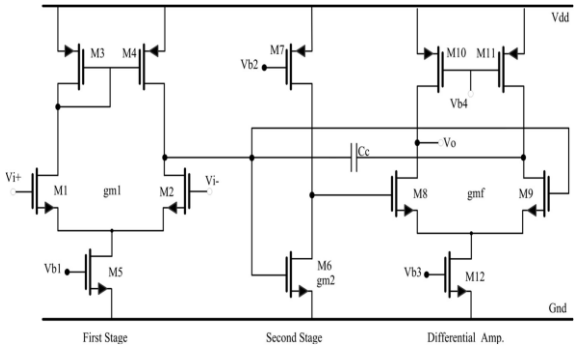
Additionally, a current comparator is incorporated into the feedback circuit. The product exhibits significant improvements in gain bandwidth, stability, and phase margin. The newly devised technique effectively enhances the performance metrics and minimizes power consumption, while significantly lowering the size of capacitors in the compensation network in comparison to alternative frequency compensation approaches that are presently available. The experimental evaluation of a three-stage amplifier has demonstrated the superiority of a novel technique in comparison to established strategies for reversed nested Miller compensation [48].In the year 2020, Francesco Centurelli conducted a study wherein he presented a paper on the attainment of double pole zero cancellation & the preference for single pole behavior of a three stage Miller capacitance amplifier. This research introduces an improved reversed nested Miller compensation technique that leverages the inclusion of a single additional feed forward stage. The proposed methodology facilitates the creation of a three-stage operational transconductance amplifier with single dominant pole and two pole-zero doublets, which are expected to exhibit theoretical cancellation. The durability of the proposed cancellation method is exemplified, as we provide evidence that variations in procedure and temperature do not affect its efficacy. The proposed design equations facilitate the determination of the resonance frequency & quality factor of the complex poles, as well as the unity gain frequency of the amplifier. In order to evaluate the performances of an operational transconductance amplifier in comparison to a telescopic cascode OTA, within specified constraints of load capacitance and power consumption, we introduce the notion of bandwidth efficiency [31].



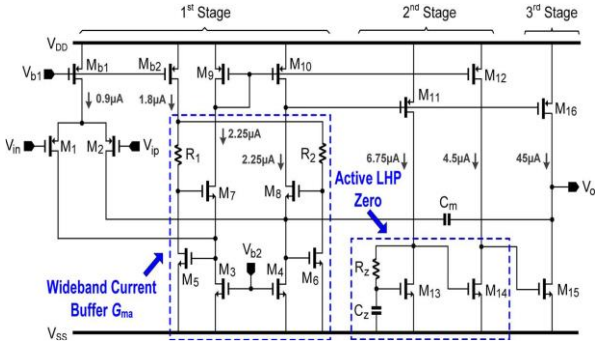
Hoi Lee in 2003 [41]



Salvatore Omar Cannizzaro in 2007 [32]



Sadegh Biabanifard in 2018 [33]



Zushu yan in 2013[34]

Table-I demonstrates a comparative analysis of the different parameters using several op-amp design techniques. The following topics are covered in this article, DC gain, power consumption, UGBW, load capacitance, settling time, slew rate, phase margin, supply voltage & area and figure 1 & figure 2 represents the histogram representation for gain and phase.

CONCLUSION

This paper presents a comprehensive analysis of the three-stage operational transconductance amplifier (OTA) architecture, encompassing wide range of advanced compensation techniques. The interpretation highlights the primary objective of the dominating design and discusses performance metrics such as gain, phase margin, power consumption, CMRR, PSRR, and so forth.

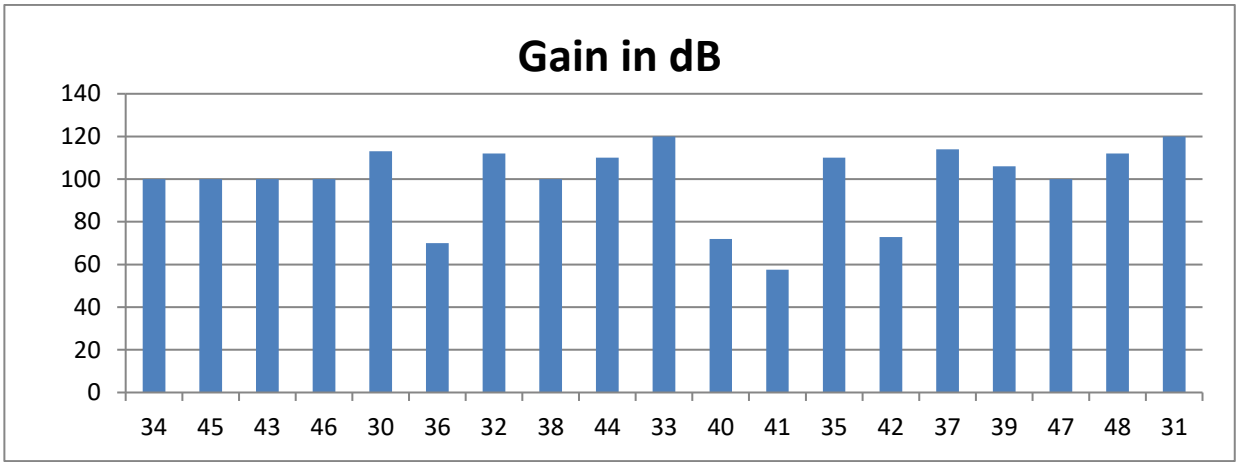


Fig 1

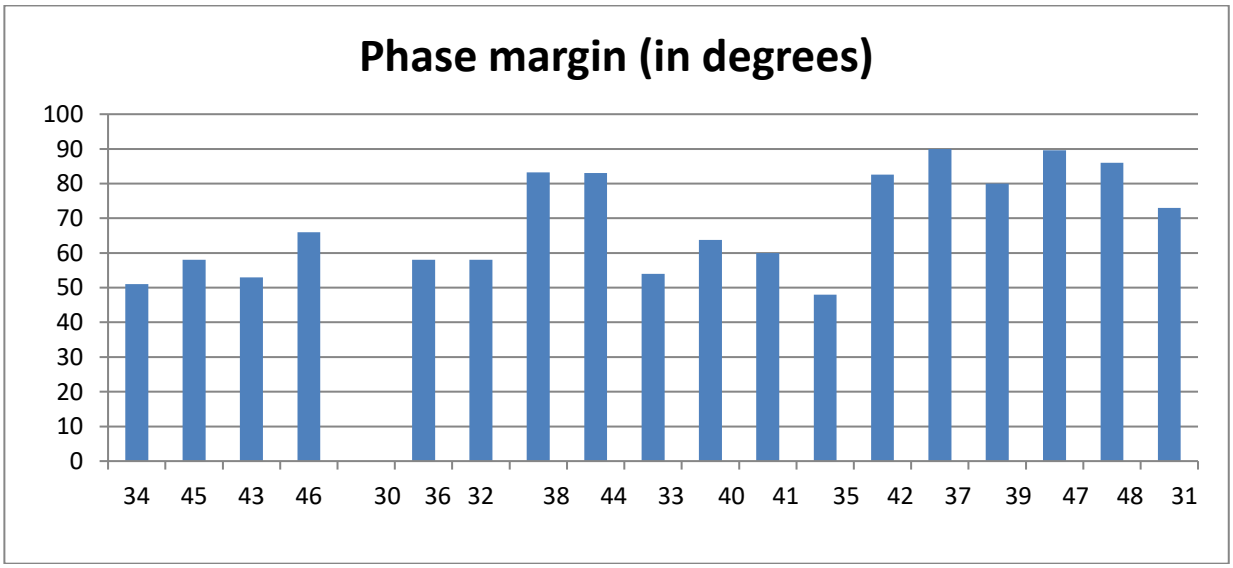


Fig 2

Author	KaNang Leung andPhilip KTMok**34**	Hoi Lee **45**	Xiaohon gPeng**43**	Feng Zhu, Shouli Yan **46**	A.D. Grasso **30**	Salvat OreOm ArCanni-Zzaro**36**	A.D. Grasso **32**	Zushu Yan **38**	Hosseini Largani **44**	A.D. Grasso **33**	Sajad Gola Bi**40**	Elena Cabre raBern al**41**	A.D. Grasso **35**	Shubin Liu **42**	Sadegh Biaba-nifard **37**	Sadegh Biaba-nifard **39**	Qi Chen g **47**	Meh di Zah ErfeKr **48**	FrancescoC enturelli **31**
Year of Publication	2001	2003	2004	2005	2006	2007	2007	2013	2014	2015	2015	2016	2017	2018	2018	2018	2019	2019	2020
Technology	500nm	.8 um	350nm	.5um	350nm	350 nm	500nm	350 nm	180nm	350nm	90nm	180nm	300nm	65nm	180nm	180nm	130 nm	180nm	130nm
Supply voltage	1v	2 v	2v	1 v	1.5 v	3 v	3 v	2 v	-	1 v	1.2 v	.7 v	1.4 v	1.2 v	1.8 v	-	1 v	1.8 v	1 v
Dc gain	100 dB	100 dB	100 dB	100 dB	113 dB	70 dB	112 dB	100 dB	110 dB	120 dB	72 dB	57.5 dB	110 dB	72.9 dB	114 dB	106 dB	100 dB	112 dB	120 dB
Power	406 uw	.4 mw	.316 mW	.36 mw	225 uW	-	.315 mw	144 uw	544 uw	195 uW	2.5 mw	25.4 uw	8.094 mw	-	360 uw	360 uw	24 uw	.285 mw	16.7 uw
GBW	1.80 MHz	4.5 MHz	1..89 MHz	2.5 MHz	1.4 MHz	22 MHz	2.4 MHz	1.37 MHz	9.08 MHz	.020 MHz	121 MHz	3 MHz	1.70 MHz	2.410 MHz	6.66 MHz	11 MHz	.92 MHz	14 MHz	24.8 MHz
Slew rate	.82/.75 v/us	1.49 v/us	.2/1.2 v/us	-	2 v/us	20.2/23.2 v/us	2.1/1.8 v/us	.59 v/us	2.23 v/us	.004 v/us	487.9 v/us	1.8/3.8 v/us	.305 v/us	17.25 v/us	1.12 v/us	.1 v/us	.62 v/us	.8 v/us	10 v/us
Phase margin	51^0	58^0	53^0	66^0	-	58^0	58^0	83.2^0	83^0	54^0	63.8^0	60^0	48^0	82.6^0	90^0	80^0	89.6^0	86^0	73^0
Load capacitance	-	120 pF	500 pF	120 pF	500 pF	-	500 pF	100 pF	100 pF	200 pF	2 pF	20 pF	10 nF	2 pF	100 pF	-	150 pF	100 pF	1 pF
CMRR	40dB	-	-	-	-	-77.4@100 KHzdB	80dB	-	-	-	-	19dB	-	-	-	-	-	-	-
Settling time	1.12/1.28us @ 1%	-	6.9/ 1.2us	-	-	53/77 ns	497/ 560	1.28 us1%	-	-	75ns @.02%	1.3/1.0 @1%	2 us	1.4 ns 1%	-	-	.15 us	-	117/105ns
Current	-	-	.158 mA	-	-	491 uA	105 uA	-	-	-	-	1.3 nA	6.36 uA	10.6 mA	-	-	-	-	-
Input voltage noise	-	-		-		10 nv/Hz	-	-	-	-	-	100 nv/Hz	-	-	-	-	-	-	-
FOM	-	1350 FOMS		-	3111 FOMS nHz/ pF/mw	-	-	9514 FOMS	1.65 FOMS	20513 FOMS MHz pF/mA	96.8 FOMS	-	-	382.5 FOMS	46.25 FOM1	740 FOM1	-	10.76 FOMS	1485 FOMS nHz/ pF/mw
FOM	-	447 FOML		-	4444 FOML v/us/Pf /mw	-	-	4097 FOML	.41 FOML	5128 FOML V F/us mA	390.3 FOML	-		273.8 FOML	1.66 FOM 2	2.44 FOM2	-	.61 FOML	598 FOMS nHz/ pF/mw
PSSR	80.75/91.94 dB @10KHz	-	-	-	-	73.6 @100 KHz dB	81 dB	-	-	-	-	52.1/64. 4dB	-	-	-	-	-	-	-
Estima Ted Area	.12 mm^2	. -	,02 mm^2	-	-	.025 mm^2	-	-	-	.004 mm^2	-	19.8 mm^2	-	-	-	-	.0036 mm^2	. -	-

REFERENCES

1. *Raj Kumar Tiwari and Gaya Prasad, "A New Circuit Model Of Low Voltage High Current Gain CMOS Compound Pair Amplifier" Published in International Journal of Electronics and Communication Engineering & Technology (IJECET), ISSN 0976 – 6464(Print), ISSN 0976 – 6472(Online), Volume 5, Issue 4, April (2014), pp. 65-71 © IAEME, Journal Impact Factor (2014): 7.2836 (Calculated by GISI)*
2. *Raj Kumar Tiwari, Gaya Prasad and Monika Tiwari, "Low Input Voltage High Gain Wideband CMOS Push-Pull Amplifier for Tuned High Pass Filter" Published in International Journal of Research in Electronics & Communication Technology, Volume-2, Issue-3, May-June, 2014, pp. 27-31, © IASTER 2014, ISSN Online: 2347-6109, Print: 2348-0017, Impact Factor: 0.7890.*
3. *Raj Kumar Tiwari, Gaya Prasad, "CMOS Compound Pair Wide Band Bio-Amplifier" Published in International Journal of Computational Engineering Research (IJCER), Vol.04, Issue 6, June-2014, pp. 57-62 ISSN (e): 2250-3005. Impact Factor: 1.145, (Computed by African Quality Centre for Journals).*
4. *Raj Kumar Tiwari, Gaya Prasad, Shiksha Jain, Ganga Ram Mishra,Monika tiwari and Parul Trivedi, "RKTG Pair Amplifier with Gain boosting stage", Published in American International Journal of Research in Science, Technology, Engineering & Mathematics, December 2018- February 2019 issue, Issue 25: Volume 1, ISSN (Print): 2328-3491, ISSN (Online): 2328-3580, ISSN (CD-ROM): 2328-3629 Impact Factor 5.01.*
5. B. Razavi, "Design of Analog CMOS Integrated Circuits", 27th ed. New Delhi: McGraw Hill Education (India) Private Limited, pp. 291- 339, 2013
6. R. Baker, "CMOS Circuit Design, Layout and simulations", 2nd ed. New Delhi: Wiley-Blackwell (an imprint of john Wiley & Sons), pp. 773-792, 2010
7. Allen, P.E., Dobkin, R. and Holberg, D.R., 2011. *CMOS analog circuit design*.Elsevier.
8. Sedra, A.S. and Smith, K.C., 2004. *Transparency Acetates for Sedra/Smith Microelectronic Circuits*.Oxford University Press.
9. Gray, P.R., Hurst, P.J., Lewis, S.H. and Meyer, R.G., 2001. Analysis and Design of Analog Integrated Circuits, JOHN WlLEY& SONS. *Inc., New York USA*.
10. Pude, M., Macchietto, C., Singh, P., Burleson, J. and Mukund, P.R., 2007, December. Maximum intrinsic gain degradation in technology scaling. In *2007 International Semiconductor Device Research Symposium* (pp. 1-2). IEEE.
11. Palumbo, G. and Pennisi, S., 2002. Design methodology and advances in nested-Miller compensation. *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications*, *49*(7), pp.893-903.
12. *Cheng, Q.; Li, W.; Tang, X.; Guo, J. Design and Analysis of Three-Stage Amplifier for Driving pF-To-nF Capacitive Load Based on Local Q-Factor Control and Cascode Miller Compensation Techniques. Electronics 2019, 8, 572.*
13. Yan, W.; Kolm, R.; Zimmermann, H. Efficient Four-Stage Frequency Compensation for Low-Voltage Amplifiers. In Proceedings of the 2008 IEEE International Symposium on Circuits and Systems, Seattle, WA, USA, 18–21 May 2008; doi:10.1109/iscas.2008.4541908.
14. *Grasso, A.D.; Palumbo, G.; Pennisi, S.; Cataldo, G.D. High-Performance Frequency Compensation Topology for Four-Stage OTAs. In Proceedings of the 2014 21st IEEE International Conference on Electronics, Circuits and Systems (ICECS), Marseille, France, 7–10 December 2014; doi:10.1109/icecs.2014.7049959.*
15. *Grasso, A.D.; Palumbo, G.; Pennisi, S. High-Performance Four-Stage CMOS OTA Suitable for Large Capacitive Loads. IEEE Trans. Circuits Syst. I Regul. Pap. 2015, 62, 2476–2484.*
16. You, F.; Embabi, S.; Sanchez-Sinencio, E. Multistage Amplifier Topologies with Nested GM-c Compensation. IEEE J. Solid-State Circuits 1997, 32, 2000–2011.
17. 17.Thandri, B.; Silva-Martinez, J. A Robust Feedforward Compensation Scheme for Multistage Operational Transconductance Amplifiers with No Miller Capacitors. IEEE J. Solid-State Circuits 2003, 38, 237–243.
18. *Biabanifard, S.; Hosseini, S.M.; Biabanifard, M.; Asadi, S.; Yagoub, M.C. Multi Stage OTA Design: From Matrix Description To Circuit Realization. Microelectron. J. 2018, 77, 49–65.*
19. Mohan, C.; Furth, P.M. A 16-W Audio Amplifier with 93.8-mw Peak Load Power and 1.43-mw Quiescent Power Consumption. IEEE Trans. Circuits Syst. II Express Briefs 2012, 59, 133–137.
20. *Yan, Z.; Mak, P.I.; Law, M.K.; Martins, R.P. A 0.016-mm2 144-_W Three-Stage Amplifier Capable of Driving 1-to-15 nF Capacitive Load with >0.95-MHz GBW. IEEE J. Solid-State Circuits 2013, 48, 527–540.*
21. Xiao, F.; Chan, P.K. A Performance-Aware Low-Quiescent Headphone Amplifier in 65-nm CMOS. IEEE J. Solid-State Circuits 2017, 52, 505–516.
22. Sung, E.T.; Park, S.; Baek, D. A Fast-Transient Output Capacitor-Less Low-Dropout Regulator using Active-Feedback and Current-Reuse Feedforward Compensation. Energies 2018, 11, 688.
23. *Marano, D.; Grasso, A.D.; Palumbo, G.; Pennisi, S. Optimized Active Single-Miller Capacitor Compensation with Inner Half-Feedforward Stage for Very High-Load Three-Stage OTAs. IEEE Trans. Circuits Syst. I Regul. Pap. 2016, 63, 1349–1359.*
24. Dhanasekaran, V.; Silva-Martinez, J.; Sanchez-Sinencio, E. Design of Three-Stage Class-AB 16 W Headphone Driver Capable of HandlingWide Range of Load Capacitance. IEEE J. Solid-State Circuits 2009, 44, 1734–1744.
25. Ochoa, A. A Systematic Approach To the Analysis of General and Feedback Circuits and Systems Using Signal Flow Graphs and Driving-Point Impedance. IEEE Trans. Circuits Syst. II Analog Digit. Signal Process 1998, 45, 187–195.

26. Lundberg, K. Internal and External Op-Amp Compensation: A Control-Centric Tutorial. In Proceedings of the 2004 American Control Conference, Boston, MA, USA, 30 June–2 July 2004;doi:10.23919/acc.2004.1384678.
27. *Grasso, A.D.; Marano, D.; Pennisi, S.; Vazzana, G. Symbolic Factorization Methodology for Multistage Amplifier Transfer Functions. Int. J. Circuit Theory Appl. 2015, 44, 38–59.*
28. *Aminzadeh, H. Evaluation of the Pole Expressions of Nano-Scale Multistage Amplifiers Based on Equivalent Output Impedance. AEU - Int. J. Electron. Commun. 2017, 72, 243–251.*
29. Shi, G. Topological Approach To Symbolic Pole-Zero Extraction Incorporating Design Knowledge. IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst. 2017, 36, 1765–1778.
30. Grasso, A.D., Palumbo, G. and Pennisi, S., 2006. Three-stage CMOS OTA for large capacitive loads with efficient frequency compensation scheme. *IEEE Transactions on Circuits and Systems II: Express Briefs*, *53*(10), pp.1044-1048.
31. Centurelli, F., Monsurrò, P., Scotti, G., Tommasino, P. and Trifiletti, A., 2020. An improved reversed miller compensation technique for three-stage CMOS OTAs with double pole-zero cancellation and almost single-pole frequency response. International Journal of Circuit Theory and Applications, 48(11), pp.1990-2005.
32. Grasso, A.D., Palumbo, G. and Pennisi, S., 2007. Advances in reversed nested Miller compensation. *IEEE Transactions on Circuits and Systems I: Regular Papers*, *54*(7), pp.1459-1470.
33. Grasso, A.D., Marano, D., Palumbo, G. and Pennisi, S., 2015. Design methodology of subthreshold three-stage CMOS OTAs suitable for ultra-low-power low-area and high driving capability. *IEEE Transactions on Circuits and Systems I: Regular Papers*, *62*(6), pp.1453-1462.
34. Leung, K.N. and Mok, P.K., 2001. Nested Miller compensation in low-power CMOS design. IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, 48(4), pp.388-394.
35. Grasso, A.D., Marano, D., Palumbo, G. and Pennisi, S., 2017. High-performance three-stage single-Miller CMOS OTA with no upper limit of ${C} _ {L} $. *IEEE Transactions on Circuits and Systems II: Express Briefs*, *65*(11), pp.1529-1533.
36. Cannizzaro, S.O., Grasso, A.D., Mita, R., Palumbo, G. and Pennisi, S., 2007. Design procedures for three-stage CMOS OTAs with nested-Miller compensation. *IEEE Transactions on Circuits and Systems I: Regular Papers*, *54*(5), pp.933-940.
37. Biabanifard, S., Largani, S.M., Biamanifard, A., Biabanifard, M., Hemmati, M. and Khanmohammadi, Z., 2018. Three stages CMOS operational amplifier frequency compensation using single Miller capacitor and differential feedback path. *Analog Integrated Circuits and Signal Processing*, *97*(2), pp.195-205.
38. Yan, Z., Mak, P.I., Law, M.K. and Martins, R.P., 2013. A 0.016-mm $^{2} $144-$\mu $ W Three-Stage Amplifier Capable of Driving 1-to-15 nF Capacitive Load With $> $0.95-MHz GBW. *IEEE journal of solid-state circuits*, *48*(2), pp.527-540.
39. 14 39. Biabanifard, S., Hosseini, S.M., Biabanifard, M., Asadi, S. and Yagoub, M.C., 2018. Multi stage OTA design: From matrix description to circuit realization. *Microelectronics journal*, *77*, pp.49-65.
40. Golabi, S. and Yavari, M., 2015. A three-stage class AB operational amplifier with enhanced slew rate for switched-capacitor circuits. *Analog Integrated Circuits and Signal Processing*, *83*, pp.111-118.
41. Cabrera-Bernal, E., Pennisi, S., Grasso, A.D., Torralba, A. and Carvajal, R.G., 2016. 0.7-V three-stage class-AB CMOS operational transconductance amplifier. *IEEE Transactions on Circuits and Systems I: Regular Papers*, *63*(11), pp.1807-1815.
42. Liu, S., Zhu, Z., Wang, J., Liu, L. and Yang, Y., 2018. A 1.2-V 2.41-GHz three-stage CMOS OTA with efficient frequency compensation technique. *IEEE Transactions on Circuits and Systems I: Regular Papers*, *66*(1), pp.20-30.
43. Peng, X. and Sansen, W., 2004. AC boosting compensation scheme for low-power multistage amplifiers. *IEEE Journal of Solid-State Circuits*, *39*(11), pp.2074-2079.
44. HosseiniLargani, S.M., Shahsavari, S., Biabanifard, S. and Jalali, A., 2015. A new frequency compensation technique for three stages OTA by differential feedback path. *International Journal of Numerical Modelling: Electronic Networks, Devices and Fields*, *28*(4), pp.381-388.
45. Lee, H. and Mok, P.K., 2003. Active-feedback frequency-compensation technique for low-power multistage amplifiers. *IEEE Journal of Solid-State Circuits*, *38*(3), pp.511-520.
46. Zhu, F., Yan, S., Hu, J. and Sánchez-Sinencio, E., 2005, May. Feedforward reversed nested Miller compensation techniques for three-stage amplifiers. In *2005 IEEE International Symposium on Circuits and Systems (ISCAS)* (pp. 2575-2578).IEEE.
47. Cheng, Q., Li, W., Tang, X. and Guo, J., 2019. Design and analysis of three-stage amplifier for driving pF-to-nF capacitive load based on local Q-factor control and cascode Miller compensation techniques. Electronics, 8(5), p.572.
48. Zaherfekr, M. and Biabanifard, A., 2019. Improved reversed nested miller frequency compensation technique based on current comparator for three-stage amplifiers. *Analog Integrated Circuits and Signal Processing*, *98*(3), pp.633-642.