Design of 243 Level Trinary Ladder Multilevel Inverter using VHDL

R. Nithya
Research Scholar, Department of Electronics and Instrumentation Engineering, Annamalai University, Chidambaram, Tamil Nadu, India, nithiazure@gmail.com

Dr. T. Anitha
Associate Professor, Department of Electronics and Instrumentation Engineering, Annamalai University, Chidambaram, Tamil Nadu, India, rgm_anitha@rediffmail.com

Dr. M. Arulaalan
Professor, Department of Electronics and Communication Engineering, C K College of Engineering & Technology, Cuddalore, Tamil Nadu, India, arulaalan@gmail.com

Abstract

In this paper, a 243 level Trinary Switched Ladder Multi-level Inverter based on a novel non-carrier switching angles algorithm is proposed. The novel switching angle algorithms generate the triggering angles for the Digital Pulse Width Modulation signals. The advantage of the non-carries switching angle algorithm is the precision of the switching signals. The Trinary Switched Ladder Multi-Level Inverter is a topology that utilizes two wings of DC sources with switch controls for the generation of the Multi-Level Inverter levels. The 243–level Trinary Switched Multi-Level Inverter requires 10 switches that split 5 each between the positive wing and negative wing respectively. The 10 switching patterns are developed using the VHDL code to control the proposed switched ladder Inverter. The validation of the proposed method is achieved using the VHDL code cross-compiled in MATLAB SIMULINK. The parameters namely %THD, Vpeak, Vrms are manipulated for the proposed 243-level Trinary Switched Ladder Multi-Level Inverter.

Keywords: *Switching Angle Generation, Ladder Inverter, Hardware Description Language, Total Harmonic Distortion.*

1 Introduction

An Inverter is a circuit that generates the AC signal from DC input. The Multi-level Inverters (MLI) are distinguished based on the switching and structure of the circuit. The MLI classification based on switching is off two types namely, Carrier-based MLI and Non-Carrier based MLI. The Carrier-based MLI is a conventional method that includes the modulating sinusoidal signal to be overlapped with the high-frequency carrier signals to generate the Pulse Width Modulation signal. The orientation of carrier signals defines the type of carrier-based method used for MLI. In contrast, the non-carrier-based MLI uses the switching angles for the control of the MLI switches. The angle generation for the switching of the MLI depends on the number of levels and topology of the Multi-Level Inverter.

Based on the number of levels, the angles of switching can be formulated for each of the quadrants of the AC output. The non-carrier switching angle algorithm is advantages in comparison to the carrier-based method for the

following reasons; i) accuracy in the generation of the triggering angles, ii) low %THD for any level of the inverter irrespective of the topology used, and iii) ease in designing using compatible digital controllers. The other aspect of the inverter classification is the topology of the circuitry.

The MLI classification based on topology depends on the type of circuitry and the number of switches used. The need for the MLI topology design is to derive the low cost, increased efficiency with the optimum number of components [1]. Though many inverters are classified based on the number of devices used, size, and design complexity; the MLI topologies have evolved by considering the reduced switch count [2]. The MLI topology with reduced switches and DC voltages is adaptable for several load-changing applications [3]. A low voltage components-based inverter topology can utilize fewer switches and DC voltages with minimum voltage stress [4]. The dual source-based MLI uses fewer power switches to operate symmetrically and asymmetrically to suit the rooftop PV application [5]. By utilizing a suitable pattern of switching devices, the staircase output can be generated with low THD% [6]. The switched ladder topology has the adaptability to various voltage ratios and the placement of DC sources with fewer power switching components [7]. The reduction in switched ladder-based MLI achieves enhanced output level helping in a smooth transition and diminished %THD [8].

To synthesize AC outputs, the Selective Harmonic Elimination is utilized to discard lower order harmonics by optimizing the switching angles of the MLI [9].The FPGA-based control for the MLI provides similarity in the %THD of both simulation and experimental results [10]. In this work, the VHDL code is developed for the design of a 243-level TSLI. The following section presents the switching angle methods and the Switched Ladder Multi-Level Inverter Topology for the development of the proposed 243-level AC output in detail.

2 Switching Angel based Trinary Switched Ladder Multi-Level Inverter

The proposed method involves the Switching Angle-based Digital Pulse Width Modulation generation for the switched ladder inverter circuit controlled by the HDL code. The AC output using the Trinary Switched Ladder Multilevel Inverter can be designed for M-levels based on the number of ladder structures used in the circuit. The angle of switching is manipulated using the formulation based on the vertical changes of levels in TSLI. Based on these angles, the Digital PWM signals are activated to control the TSL-MLI. The Trinary Switched Ladder topology uses the ladder structure for the switches and consists of two wings of switched ladders namely positive ladder structure and negative ladder structure. The number of levels decides the number of ladders and thus the switch count for the TSL-MLI circuit.

A) Switching Angle Algorithm

The switching angle algorithms are utilized for the triggering of Digital PWM generation to be used in the TSLI. The switching angles are generated using the mathematical equation. There are four types of switching angle algorithms namely Equal Phase Method, Half Equal Phase Method, Feed Forward Method, and Half Height Method. Among the four switching angle algorithms, the HH-SAA is best suitable for the MLI generation since the THD% is low. The switching angles are assigned with equal space till the 50% of the multi-level inverter output and with equal space in alternate angles above the 50% of the multi-level inverter output. The mathematical equation for the HHM is given in equation (1) as

$$\alpha_i = sin^{-1}\left[\left(i-\frac{1}{2}\right)\frac{2}{N-1}\right] = sin^{-1}\left[\frac{2i-1}{N-1}\right] \quad (1)$$

$$where\ i = 1, 2, \ldots, \frac{N-1}{2}$$

The switching angles are generated for all four quadrants of the required AC output of the MLI. The N-level MLI circuit will consist of N–1switching angles for each of the quadrants. The calculations of switching angles in all quadrants are interlinked.

B) Trinary Switched Ladder Topology

In the Trinary SLI circuit, the MOS transistors are arranged in the ladder format as depicted in Fig.1. The TSLI consists of two sections of the circuitry such as the Positive section and Negative section. As shown, the section above the ground terminal is referred to as Positive Section and the section below the ground terminal is referred to as the Negative Section. In other words, the positive section includes the positive voltages of the inverter and the negative section includes the negative voltages of the inverter. The control of the associated switches of the proposed inverter defines the levels of the AC output. Based on the orientation of DC source values, the switched ladder inverter can be classified as a Symmetrical Switched Ladder Inverter and Asymmetrical Switched Ladder Inverter. The Symmetrical Ladder Inverter uses the same value of DC for all the stages, whereas the asymmetrical Ladder Inverter utilizes different values of DC for all the stages. The Asymmetrical Switched Ladder MLI can be classified into several types based on the type of progression used in the DC source values such as Binary SLI, Modified Binary SLI, Luo Progression SLI, Ye Progression SLI, and Trinary SLI. As shown in Table 1, the Trinary Switched Ladder MLI is advantageous compared to the other Switched Ladder types in terms of the number of switches used, the number of stages in design, Number of DC sources for the maximum levels of the inverter. By using the same number of switches and stages in Switched Ladder configurations, the maximum level of 243 is achieved for the Trinary Switched Ladder Topology and proves to be advantageous compared to the other Ladder inverter topologies to the inverter characteristics.

Table 1. Comparison of Inverter characteristics for different Switched Ladder Topologies

Inverter	Binary Ladder Inverter	Luo Ladder Inverter	Ye Ladder Inverter	Trinary Ladder Inverter
No. of Switches	10	10	10	10
Number of Stages	10	10	10	10
Number of DC sources	10	10	10	10
Total number of Levels	63	189	225	243

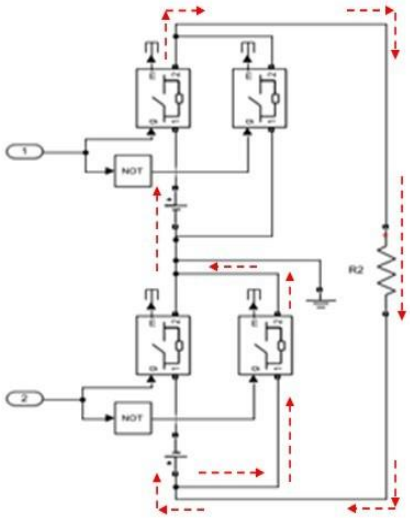
The operation of the Switched Ladder MLI is important for the generation of switching DPWM. As discussed, the SLI utilizes two wings of the Ladder to generate the required AC output. The direction of current flow for the positive wing and negative wing for the 3-level TSLI is shown in Fig. 1. For the positive DC voltage to pass through the load, the direct switch1 has to be “ON” and complementary of switch 2 should be “ON”. Simultaneously, the complementary switch 1 and direct switch 2 should be "OFF" as depicted in Fig.1(a).

Similarly, for the negative DC voltage to pass through the load; the complementary switch1 and direct switch2 should be “ON” with the direct switch1 and complementary switch2 should be OFF as depicted in Fig. 2(b). Depending on the value of the level in the MLI, the switches operate in patterns to accomplish the AC output response. The DC voltages sources of the proposed ladder inverter use the trinary sequence of voltage values such as 1V, 3V, 9V, and 27V. The mathematical equation for the proposed TSLI is represented as given in equation (2)

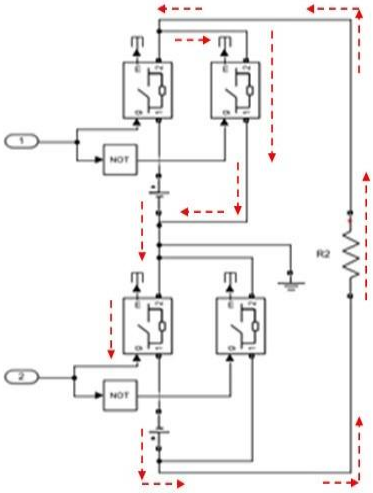
$$E_{DCN} = 3^N E \qquad (2)$$

Where N = number of Levels; E = voltage

Fig 1. Current flow for the proposed Switcher Ladder Multi-Level Inverter



a

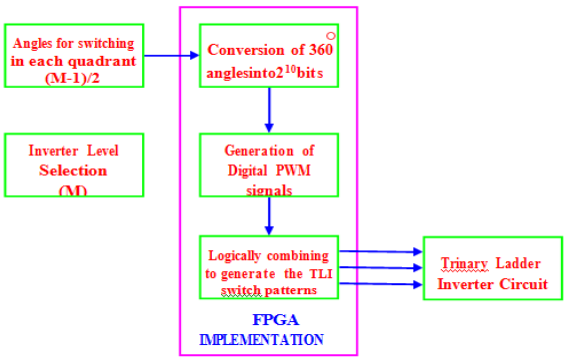


b

3 The proposed 243-level Trinary Switched Ladder Inverter: Methodology

This work proposes the design for the 243-level TSL Multi-level Inverter utilizing the VHDL code. The switching of the TSLI circuits is controlled by the Digital PWM signals that are formulated using the Half Height-Switching Angle Algorithm. The HH-SAA provides an accurate manipulation of the angles at which the levels have to change as per the AC output of the 243-level TSLI. Fig. 2 depicts the block diagram representation of the proposed 243-level TSLI using the VHDL code. The first step in the design is the selection of the number of levels in the TSLI. Based on the number of levels selected, the switched ladder stages can be derived for the TSLI. For the 243- level, the five switched ladder stages are required at both positive and negative sections of the TSLI. Also, the number of switches is 10 for the proposed 243-level TSLI. The switching angles are manipulated for the 10 switches in the four quadrants using the mathematical formulation of HH- SAA. The derived values are converted into 210-bit equivalence to develop the VHDL code. The bit equivalent values for the 10 switches are utilized for the ON & OFF time instances of the Digital PWM signals. The switching patterns are generated by logically combining the Digital PWM signals as per the 243-level TSLI circuit. The VHDL code generated 10 switch patterns are connected to the TSLI circuitry by the System generator cross-compiler.

Fig 2. Block diagram for the proposed 243 level Trinary Switched Ladder Multi-Level Inverter



A) Switching Angle Algorithm for 243-Level TSLI

The 243 level TSLI output is generated by using the non-carrier SA Algorithm namely Half Height SAA. For the 243 levels, the HH-SAA generates the 121 DPWM angles in the

positive and negative parts of the AC output with a zero level. Within 180°, the HH-SAA generates rising edge and falling edges for the 121 DPWM signals. Also, in the next half-cycle (180° – 360°), the HH-SAA produces rising and falling edges for the 121 DPWM signals. Overall, 484 angles are digitized to develop the VHDL code. The resolution for the proposed HH-SAA is fixed at 210 bits. Table 2 represents the digitized equivalent for the angles of the AC output.

Table 2. Digitized equivalence for the Angles of the AC output

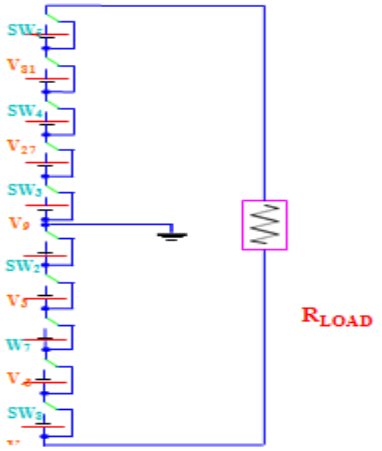
Angles	Digitized Equivalent
First(0°–90°)	0 – 256
Second (90°–180°)	256 – 512
Third (180°–270°)	512 – 768
Fourth (270°–360°)	768 – 1024

B) Topology of 243-Level Trinary Switched Ladder Multi-Level Inverter

For the 243 level TSLI circuit, there are five ladder stages on both wings (positive and negative) of the ladder. The DC voltages values for the five ladder stages are assigned in Trinary progression namely 1V, 3V, 9V, 27V, and 81V respectively for both the forward bias of the positive wing and the reverse bias of the negative wing as shown in Fig.3.

To generate the 243 level AC output, the switches are controlled from 0 to 121 to 0 levels in the positive cycle and 0 to -121 to 0 levels in the negative cycle of the AC output. The voltage combination for the 243-level TSLI is derived from the ternary input DC voltages for each level. The DC voltage combinations for the 243 levels are unique for the respective levels as per the manipulation of the DC sources. The patterns for the 243 levels require the 10 switches to be configured according to voltage fusion of the positive cycle and negative cycle of the TSLI output.

Fig 3. Circuit diagram for the proposed 243-level Trinary Switched Ladder Multi-Level Inverter



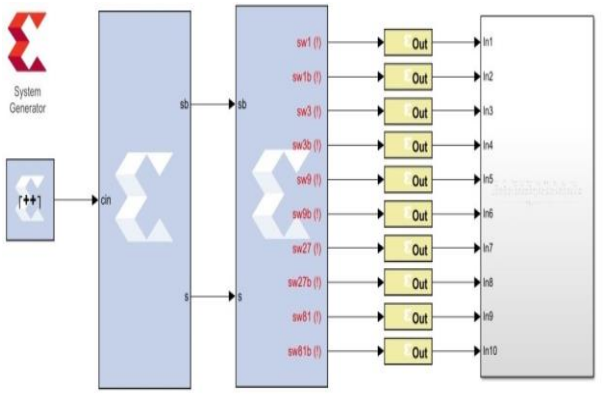
4 Results And Discussions

The proposed 243–level TSLMLI is developed and simulated using the MATLAB SIMULINK cross-compiled with the System Generator as shown in Fig. 4. The VHDL code for the 242 DPWM signal generations is achieved by the behavioral style of coding using the 210-bit equivalence for the switching angles. The 242 DPWM signals are declared as array signals represented as “S” and “Sb” as shown. Fig.5 depicts the switch patterns of the proposed method for 243 levels. The cross-compiling of the VHDL code is accomplished by making use of the black box in the System Generator tool.

The MATLAB tool evaluates the parametric analysis namely THD%, Vrms, and Vpeak for the proposed 243-level TSLI. The AC output voltage of the 243 level TSLI is depicted in Fig. 6(a) with a resolution of 210 bits. The %THD for the proposed 243 level TSLI is shown in Fig. 6(b). The %THD value is as low as 1.78% for the presented 243 level TSLI circuit. Fig 7 depicts the power dissipation of the proposed 243-level TSLI VHDL code for the switching pattern generation. The power dissipation is evaluated at the two phases namely before synthesis and after synthesis that changes both

dynamic and static power dissipation of the proposed method.

Fig 4. MATLAB SIMULINK Model for the proposed 243-level TSLI using System Generator Tool



The proposed topology is compared with the existing topology to identify that the highest level of MLI is attained with the fewer number of components and the cost of the topology is fixed at 69.5$ as presented in Table 3. Also, the Component count per level factor is as low as 0.082. In comparison, the parametric analysis of the proposed method is better than the existing methods as given in [11][12][13][14]. Table 4 presents the Device Utilization for the proposed method using the Artix7 FPGA device. Table 5 shows the timing delay of the inverter switches and maximum delay occurs with SW1 due to the presence of 8 levels in the design. The 243-level TSLI AC output has to be generated at the frequency of 50 Hz. Conventionally, the frequency of the carrier signal is considered for the switching frequency. In this work, the non-carrier switching angles are utilized for the generation of the DPWM that consists of a switching frequency say 20 kHz. The scaled-down value for the proposed 243-level TSLI is 195. To scale down the frequency to 50 Hz, the switch patterns are to be manipulated based on equation (3)

$$Scaled\_down\_value = \frac{1}{2^{10} X\ 50Hz\ X\ 100ns} \quad (3)$$

where 100ns is the clock period; 50Hz is the AC output frequency.

Fig 5. DPWM based Switch Patterns of the proposed 243-level TSLI using MODEL SIM tool

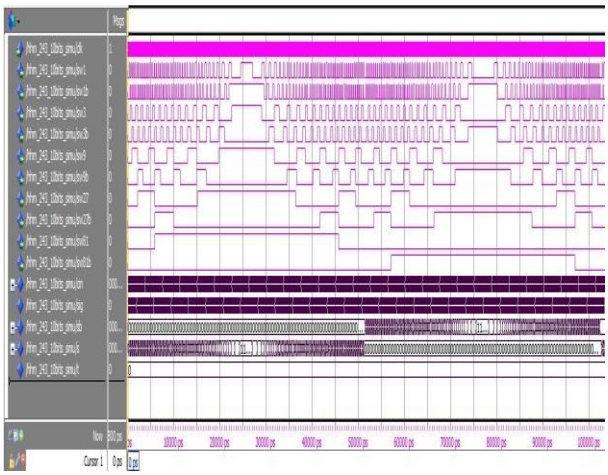
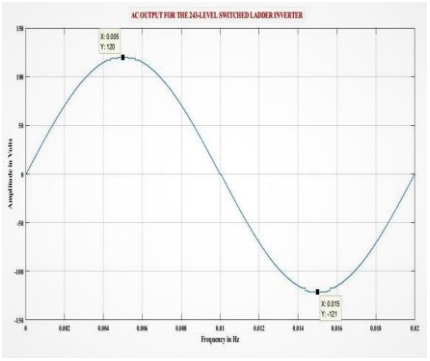
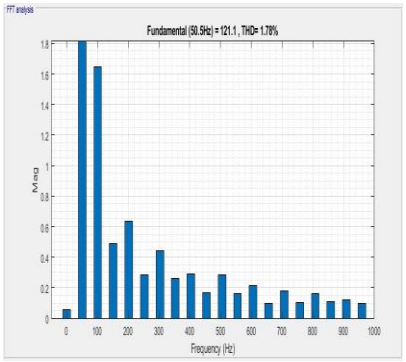


Fig 6. (a) Simulated AC output and (b) %THD for the proposed 243-level Trinary Switched Ladder Multi-Level Inverter

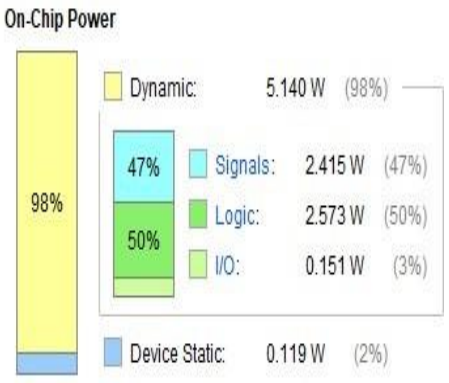


a

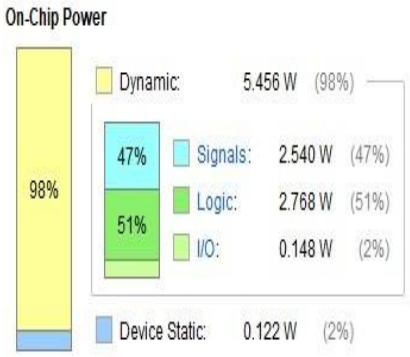


b

Fig 7. On-Chip Power Calculation for the proposed 243-level TSLI using Artix-7 FPGA



a



b

Table 3. Comparison of various Multi-Level Inverters with the proposed 243-level TSLI

Topology	[11]	[12]	[13]	[14]	Proposed
Number of Switches	20	10	12	10	10
Number of Diodes	--	10	10	--	--
Number of Capacitors	--	3	--	--	--
Number of DC sources	--	6	3	3	10
Level of the MLI	81	21	21	21	243
Overall Cost in $	139	--	--	--	69.5
Component count per level factor "Fccl"	--	1.86	1.2	1.1	0.082

Table 5 Timing Delay Analysis for the Control switches of the Inverter using the (xc7a100tcsg324-1) Artix-7 family device

Resource	Utilization	Available	Utilization %
LUT	665	63400	1.05
FF	17	126800	0.01
IO	11	210	5.24
BUFG	1	32	3.13

	Slack ^1	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Logic %	Net %
Path 11	∞	8	8	172	cin_reg[8]/C	SW1	10.021	4.027	5.994	40.2	59.8
Path 12	∞	8	8	172	cin_reg[8]/C	SW1b	10.006	4.027	5.979	40.2	59.8
Path 13	∞	8	8	121	cin_reg[5]/C	SW3	9.150	4.027	5.123	44.0	56.0
Path 14	∞	8	8	123	cin_reg[6]/C	SW9	9.081	4.027	5.054	44.3	55.7
Path 15	∞	7	7	130	cin_reg[4]/C	SW3b	9.021	3.929	5.092	43.6	56.4
Path 16	∞	7	7	172	cin_reg[8]/C	SW27	8.889	3.903	4.986	43.9	56.1
Path 17	∞	8	8	105	cin_reg[7]_rep/C	SW9b	8.794	4.027	4.767	45.8	54.2
Path 18	∞	7	7	145	cin_reg[1]/C	SW27b	8.506	3.927	4.579	46.2	53.8
Path 19	∞	4	4	121	cin_reg[5]/C	SW81	6.200	3.555	2.645	57.3	42.7
Path 20	∞	4	4	135	cin_reg[10]/C	SW81b	6.056	3.557	2.499	58.7	41.3

5. Conclusion

The proposed 243-level Trinary Switched Ladder Multi-Level Inverter is evaluated successfully using the VHDL cross-compilation in MATLAB SIMULINK. The performance of the proposed method is validated and found to be satisfactory with the %THD as low as 1.78%. Also, the proposed topology is meritorious with the respect to the number of components utilized, Cost function, and device utilization in the FPGA device. Future work can be directed towards the implementation of the 243-level Trinary Switched Ladder Multi-Level Inverter.

References

W AlaaeldienHassan , Xu Yang, Wenjie Chen and Mohamad Abou Houran, "A State of the Art of the Multilevel Inverters with Reduced Count Components", Electronics, MDPI, Vol. 9,2020.

Hari Priya Vemuganti ,DharmavarapuSreenivasarao, Ganjikunta Siva Kumar, Hiralal M Suryawanshi, Haitham Abu Rub, "A Survey on Reduced

Switch Count Multilevel Inverters", IEEE Open Journal of the Industrial Electronics Society, 2021.

M. JagabarSathik, Dhafer Almakhles, S. Ahamed Ibrahim, Saeed Alyami, S. Sivakumar, Mahajan Sager Basker, "A Generalized Multilevel Inverter Topology with Reduction of Total Standing Voltage", IEEE Access,2017.

MarifDaula Siddique, Saad Mekhilef, MuhyaddinRawa, Addy Wahyudie, BekkhanChokaev, and Islam Salamov, "Extended Multilevel Inverter Topology With Reduced Switch Count and Voltage Stress", IEEE Access,2020.

Prem Ponnusamy, PandarinathanSivaraman, Dhafer J. Almakhles, SanjeevikumarPadmanaban, Zbigniew Leonowicz, MatheswaranAlagu, and JagabarSathik Mohamed Ali, "A New Multilevel Inverter Topology With Reduced Power Components for Domestic Solar PV Applications", IEEE Access,2020.

Prabhat Ranjan Bana, Kaibalya Prasad Panda, R. T. Naayagi, PierluigiSiano, and Gayadhar Panda, "Recently Developed Reduced Switch Multilevel Inverter for Renewable Energy Integration and Drives Application: Topologies, Comprehensive Analysis and Comparative Evaluation", IEEE,2019.

Kannan Chandrasekaran, Nalin Kant Mohanty, "A Flexible Rung Ladder Structured Multilevel Inverter" ,Tehničkivjesnik, 2020.

VishwajithN , S Nagaraja Rao and Sachin S, "Performance analysis of reduced switch ladder-type multilevel inverter using various modulation control strategies", Journal of Physics: Conference Series, 2020,pp:1-12.

MarifDaula Siddique, Atif Iqbal, Mudasir Ahmed Memon, and Saad Mekhilef, "A New Configurable Topology for Multilevel Inverter with Reduced Switching Components", IEEE Access, 2017,pp:1-15.

Guido Ala , Massimo Caruso, Rosario Miceli, Filippo Pellitteri, Giuseppe Schettino, Marco Trapanese and Fabio Viola, "Experimental Investigation on the Performances of a Multilevel Inverter Using a Field Programmable Gate Array-Based Control System", Vol. 12, Energies, MDPI, 2019,pp:1-17.

Ganesh Kumar Srinivasan, Marco Rivera ,Vijayaraja Loganathan, Dhanasekar Ravikumar and Balaji Mohan "Trends and Challenges in Multi-Level Inverter with Reduced Switches", Electronics, MDPI, Vol.10, 2020,pp:1-23.

S. T. Meraj, N. Z. Yahaya, K. Hasan, and A. Masaoud, "Single phase 21 level hybrid multilevel inverter with reduced power components employing low-frequency modulation technique," vol. 11, International Journal of Power Electronics Drive System, 2020.

S. Sabyasachi, V. B. Borghate, and S. K. Maddugari, ''A 21-level bipolar single-phase modular multilevel inverter,'' Journal of Circuits, Systems and Computers, vol. 29,2020.

Shaik ReddiKhasim, Dhanamjayulu C, SanjeevikumarPadmanaban, Jens Bo Holm-Nielsen, And Massimo Mitolo, "A Novel Asymmetrical 21-Level Inverter for Solar PV Energy System With Reduced Switch Count", Vol. 9, IEEE Access, 2020,pp:11761-11775.